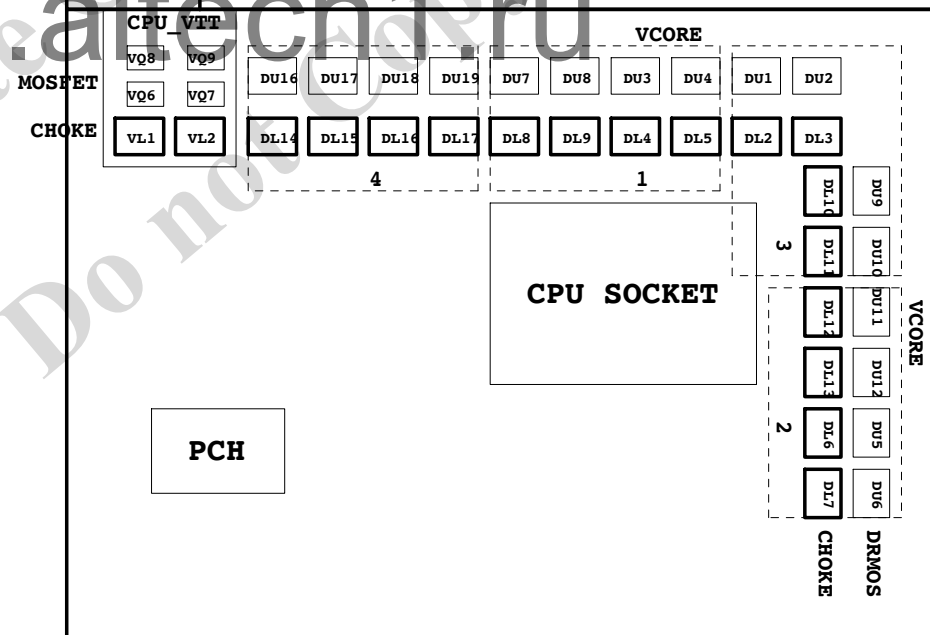


Rev 1.02

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT_3
15	PCI EXPRESS*16/*8 SWITCH_2
16	PCI EXPRESS*8 SLOT_2
17	PCI EXPRESS*16 SLOT_1
18	PCI EXPRESS*16/*8 SWITCH_1
19	PCI EXPRESS*8 SLOT_1
20	PCI EXPRESS*1 SLOTS X1
21	HDMI/DVI/DP
22	Dual BIOS , TPM SLB9635TT
23	CT9570 AUDIO
24	REAR AUDIO JACK
25	AUDIO power
26-28	IR 3563A+IR3550-Vcore
29	DISCRETE POWER1
30	DISCRETE POWER2
31	ITE 8728 LPC IO
32	FP,FUSB,-PHOT
33	ATX POWER, CLOCK GEN
34	HWM,KB/MS , FAN CTRL
35	INTEL LAN I217
36	INTEL LAN I210
37	Marvell 9230
38-39	IR3570A+IR3598-DDR15 POWER

SHEET	TITLE
40	RST, PWR, CLR_CMOS
41	PEX8747S UPSTREAM & MISC
42	PEX8747S DOWNSTREAM SLOTS
43	PEX8747S STRAP & CPLD INTF
44	PEX8747S POWER
45	REFCLK
46	PEX8747 POWER DESIGN
47	IT8790
48	FAN CTRL
49-51	D720210 4port_Hub - Rear
52-54	D720210 4port_Hub - Front
55	TABLE LIST



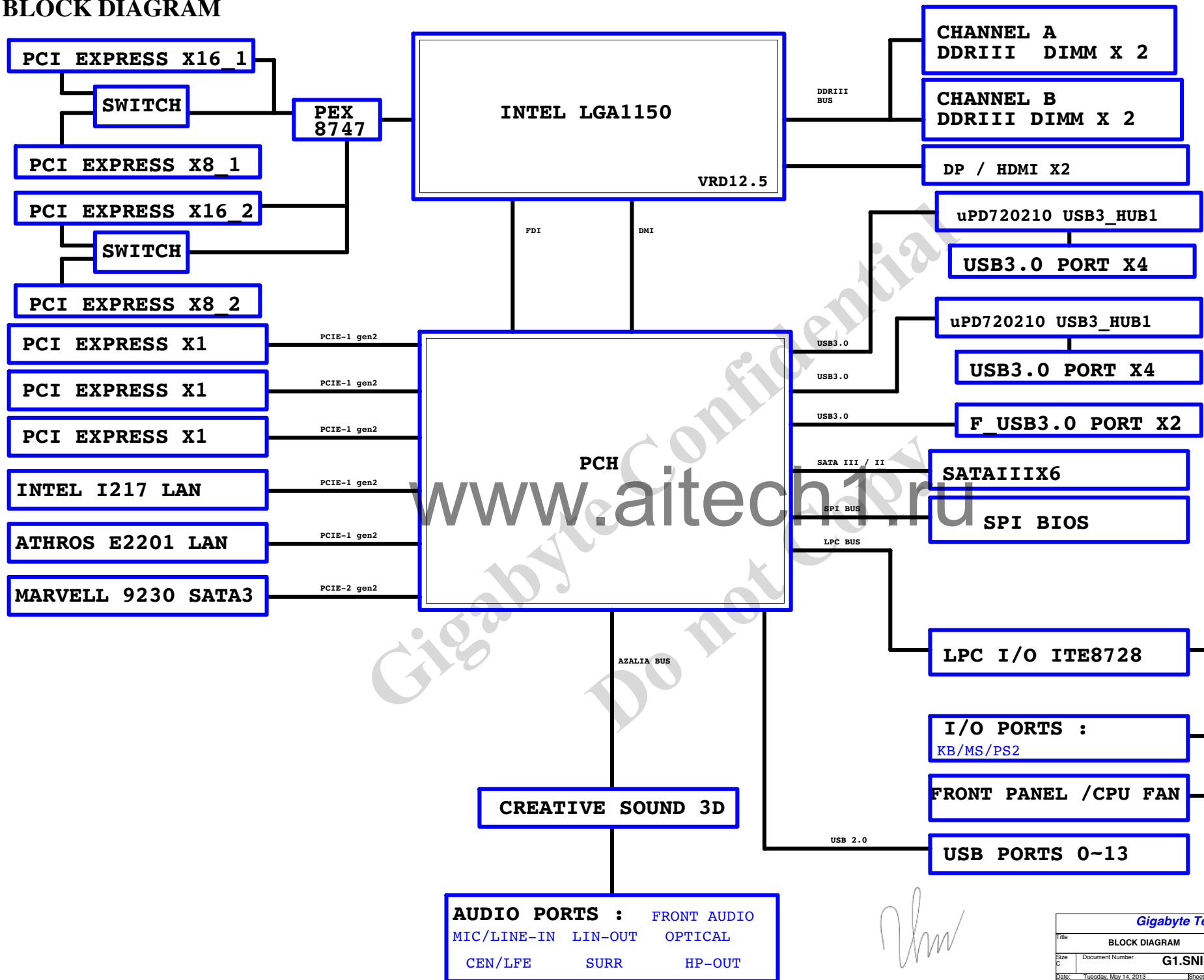
Gigabyte Technology

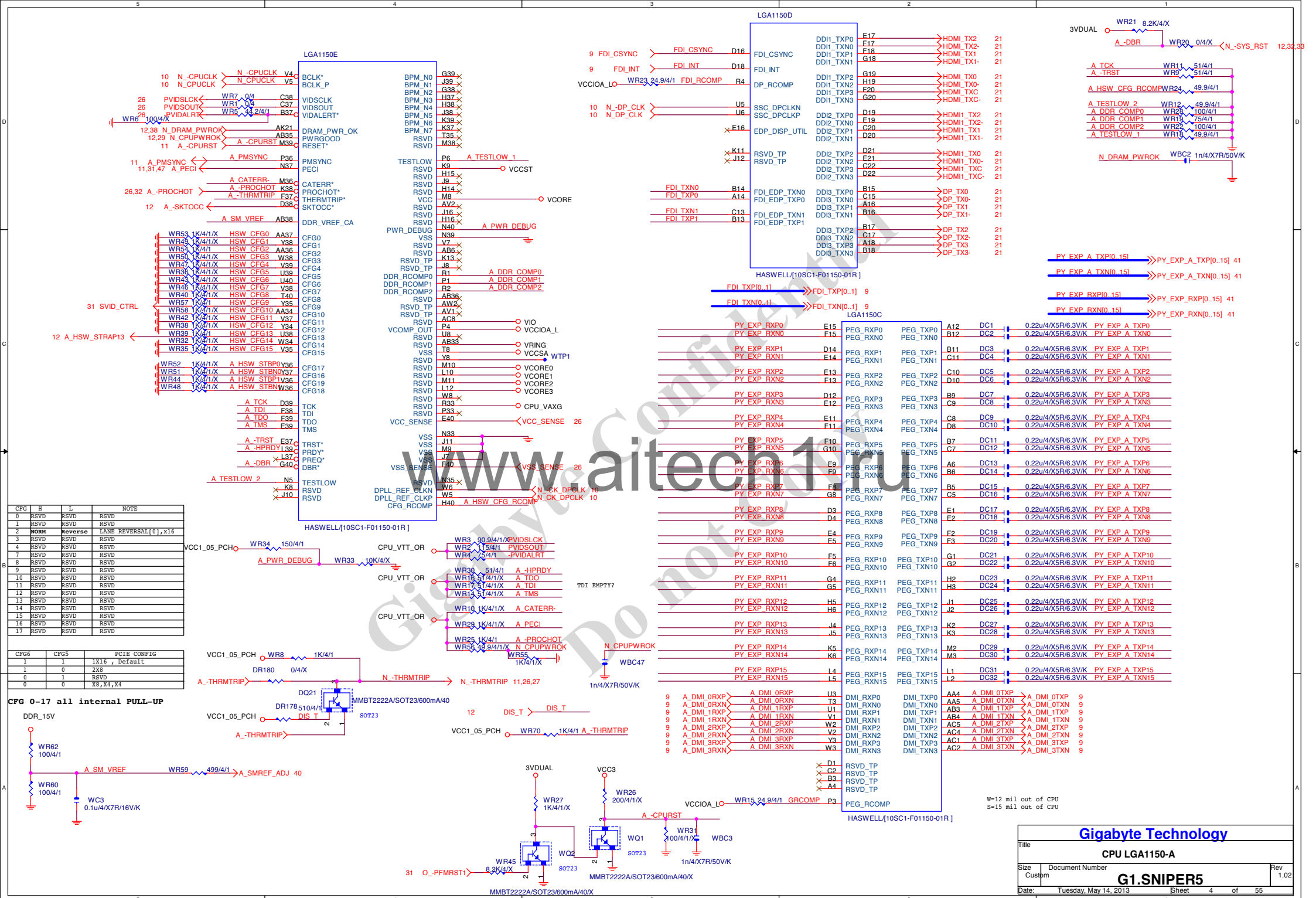
Component value change history

[illegible]

DATE	Change Item	Reason
2012/3/25	0.1-EBOM	
2013/02/23	修改 VIOA.VSA零件名稱 修改快充線路 ADD ADUIO LED N_GPIO37 Add pu hi 3vdual	
2013/03/28	7.0B 修改HUB線路	
2013/04/02	1.01B 修改文字面.及OTP線路	
2013/04/08	1.02B 修改文字面	

BLOCK DIAGRAM



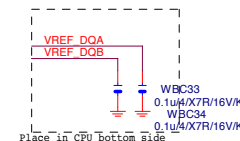


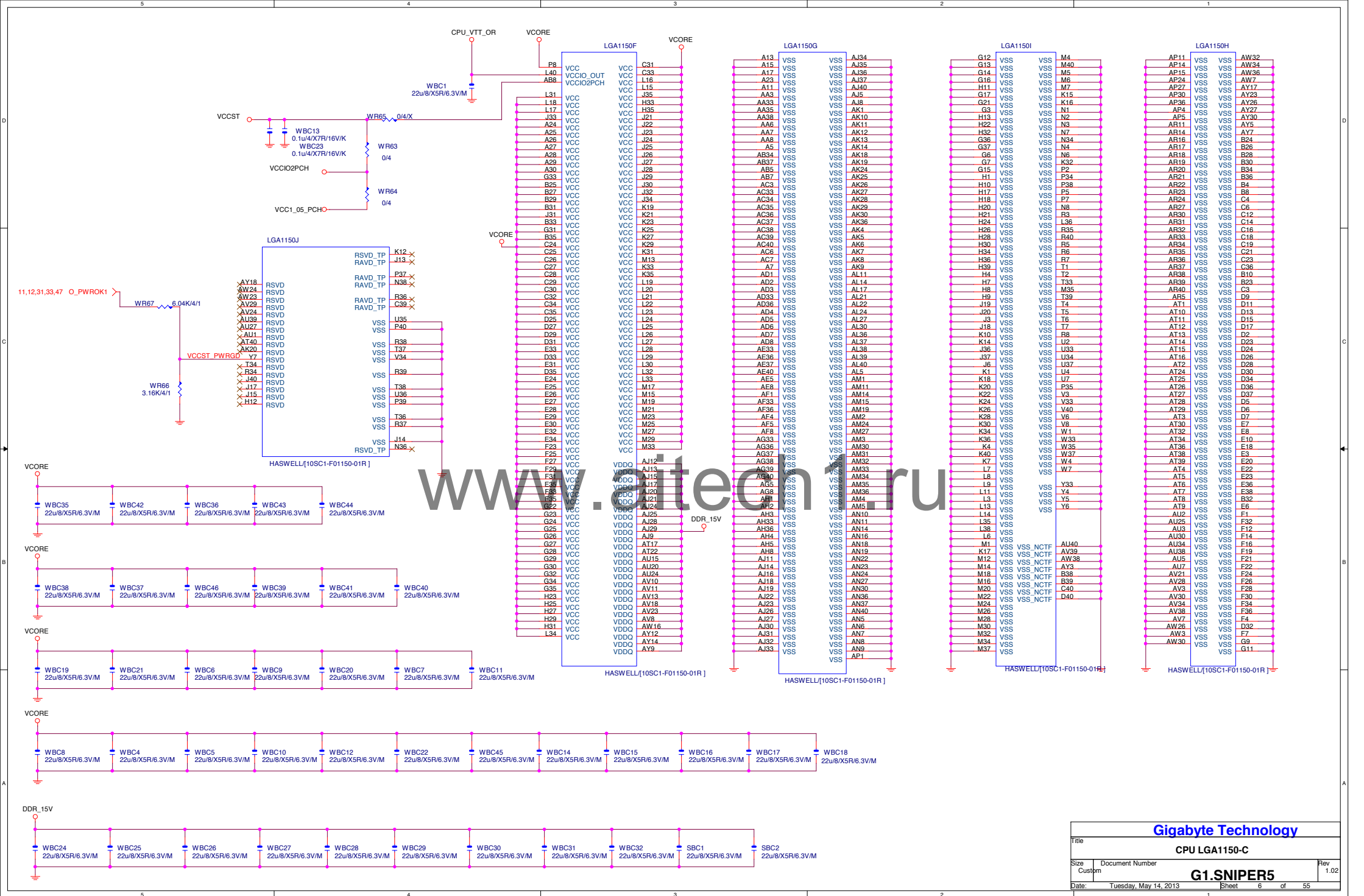
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0.1u/4/X7R/16V/K/X

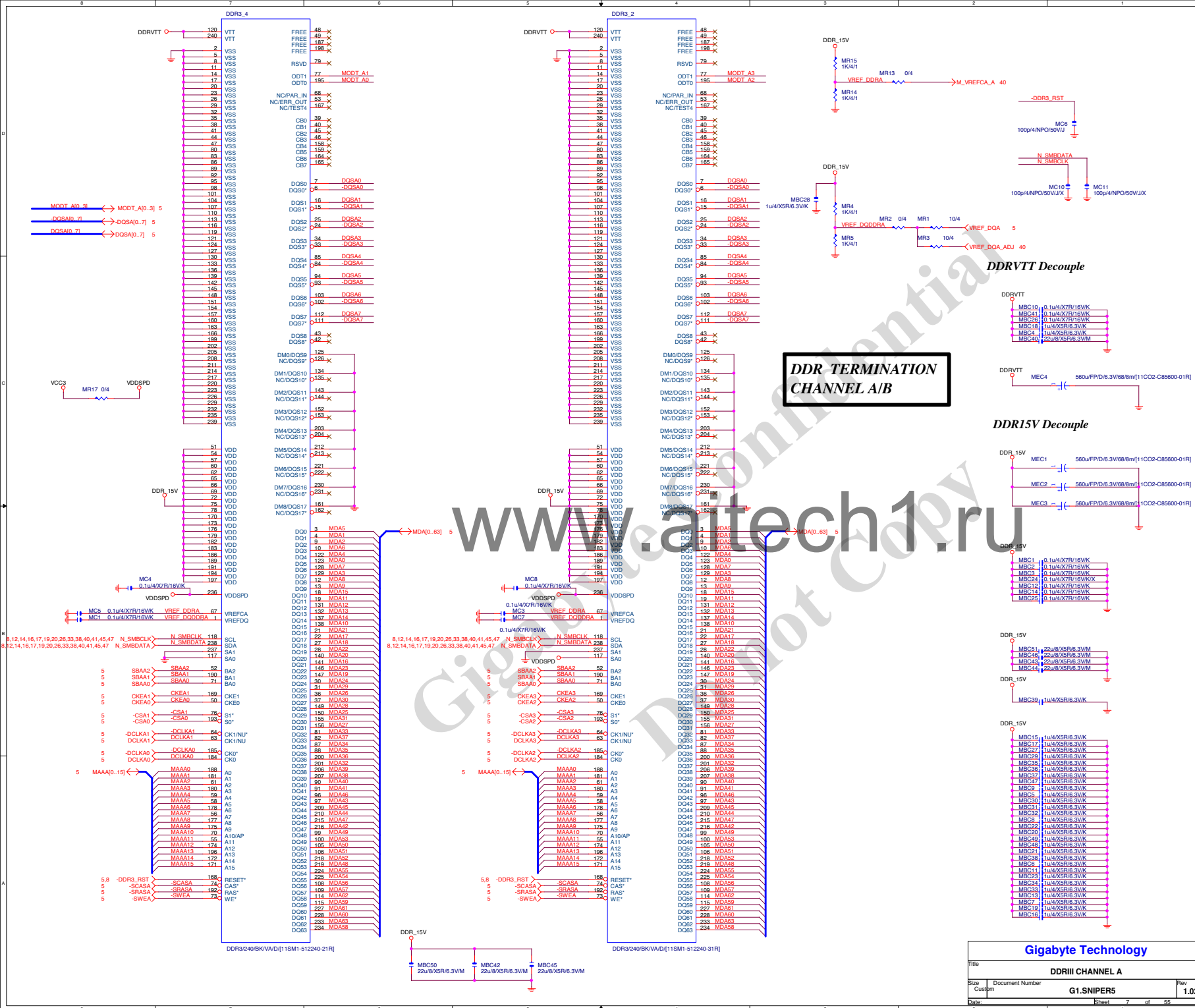
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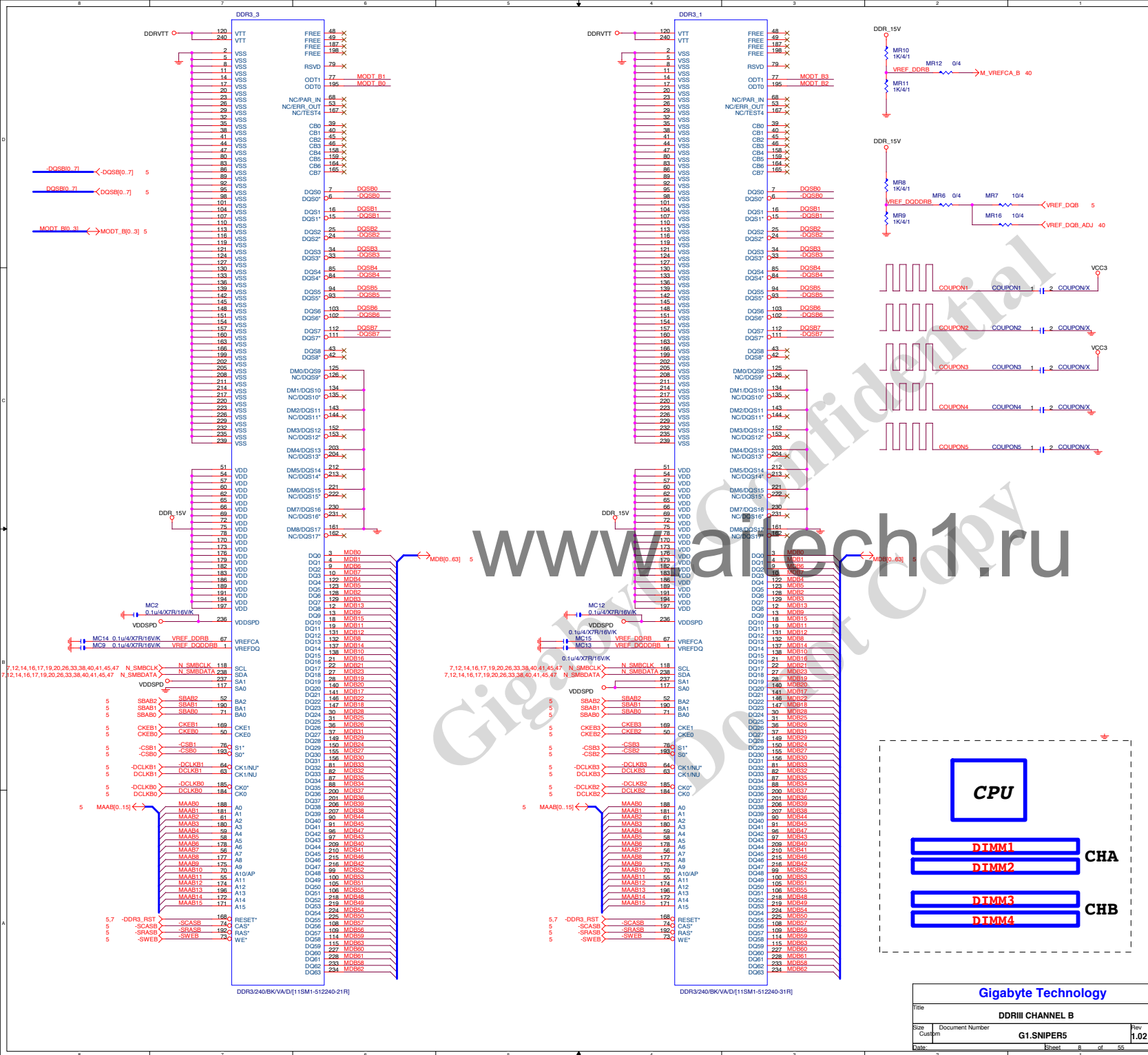


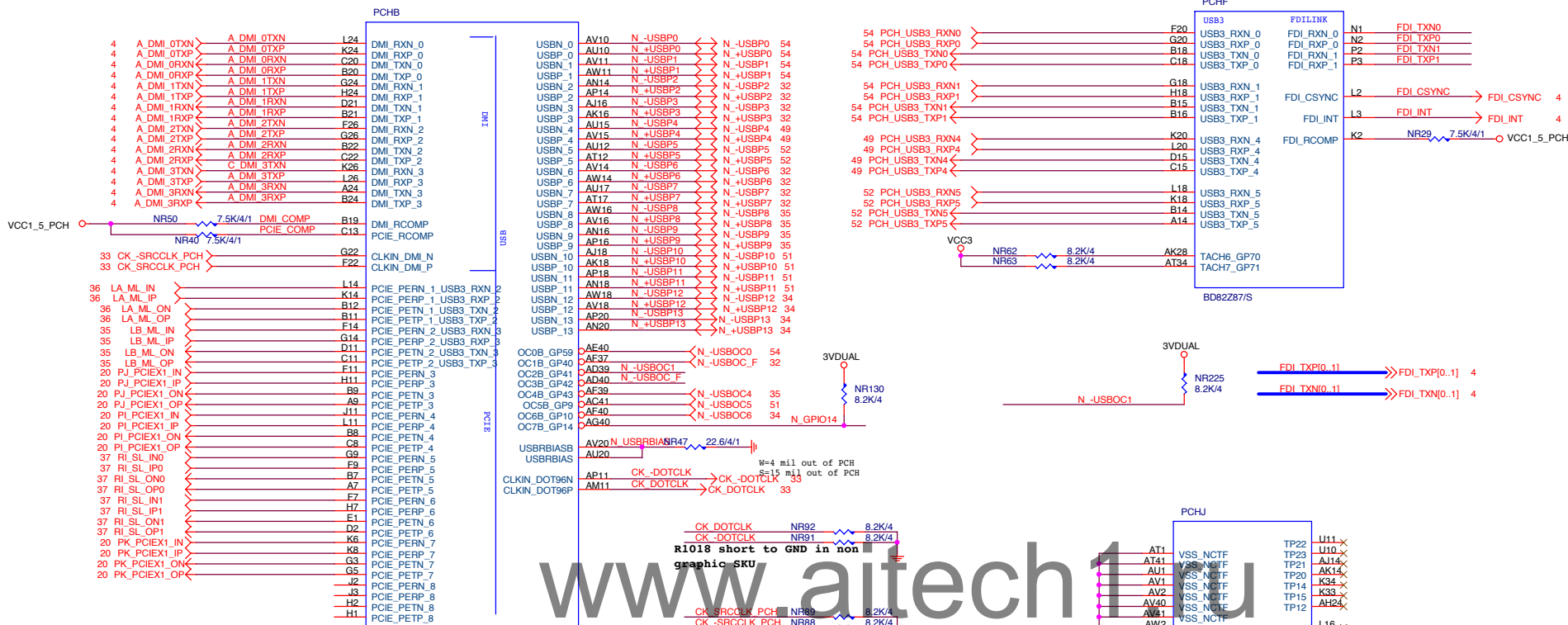
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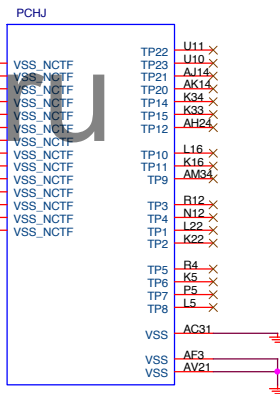
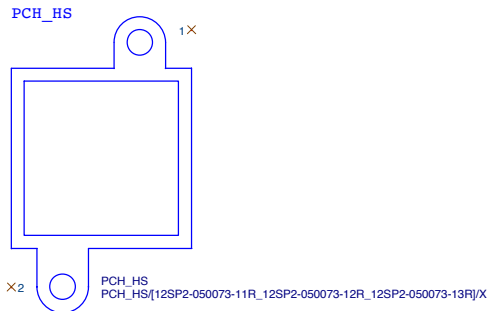




PCIEX1:16/5/5/16 (breakout min 8/4/4/4/8)

Impedance=80 +- 17.5%

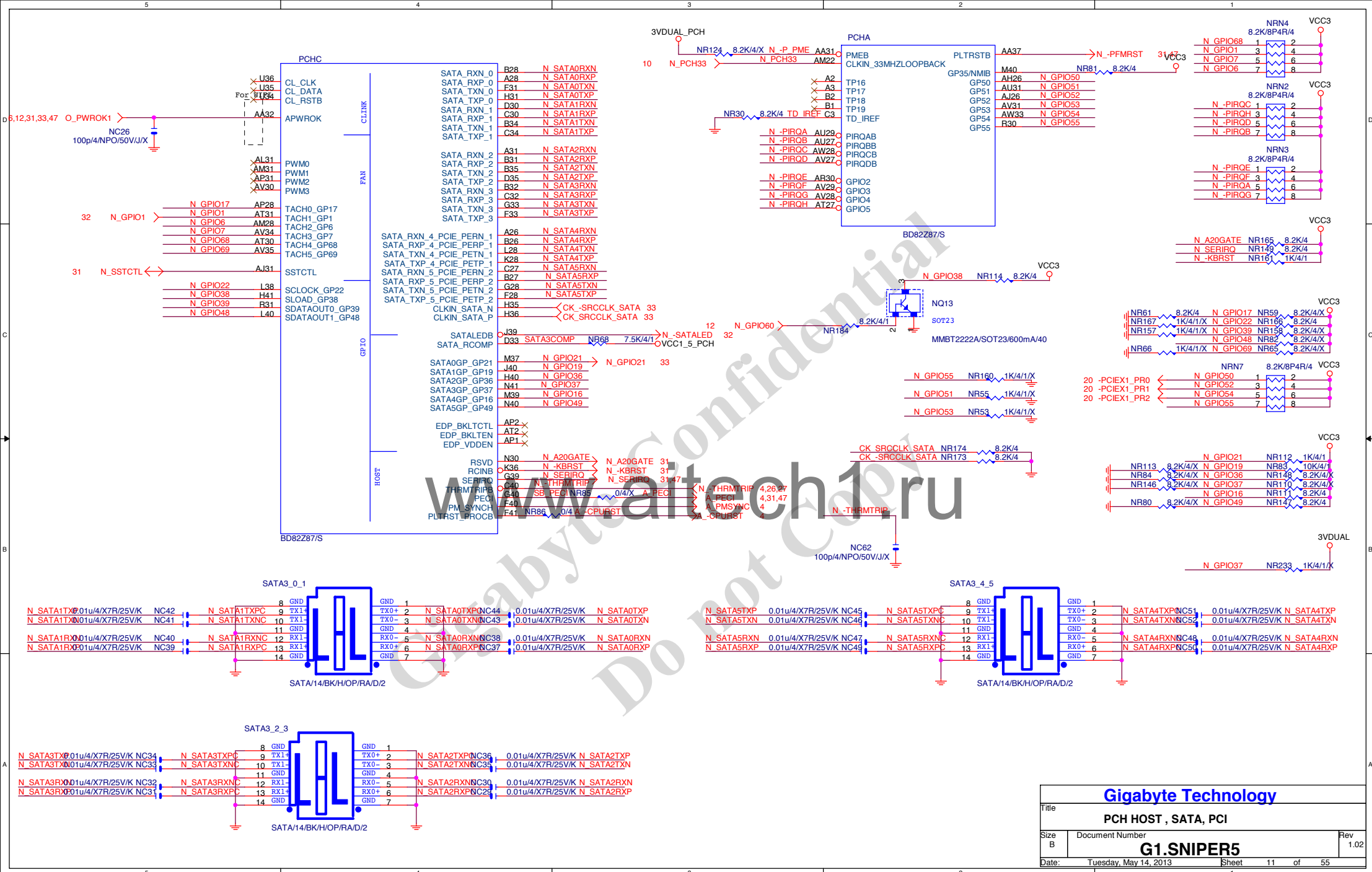
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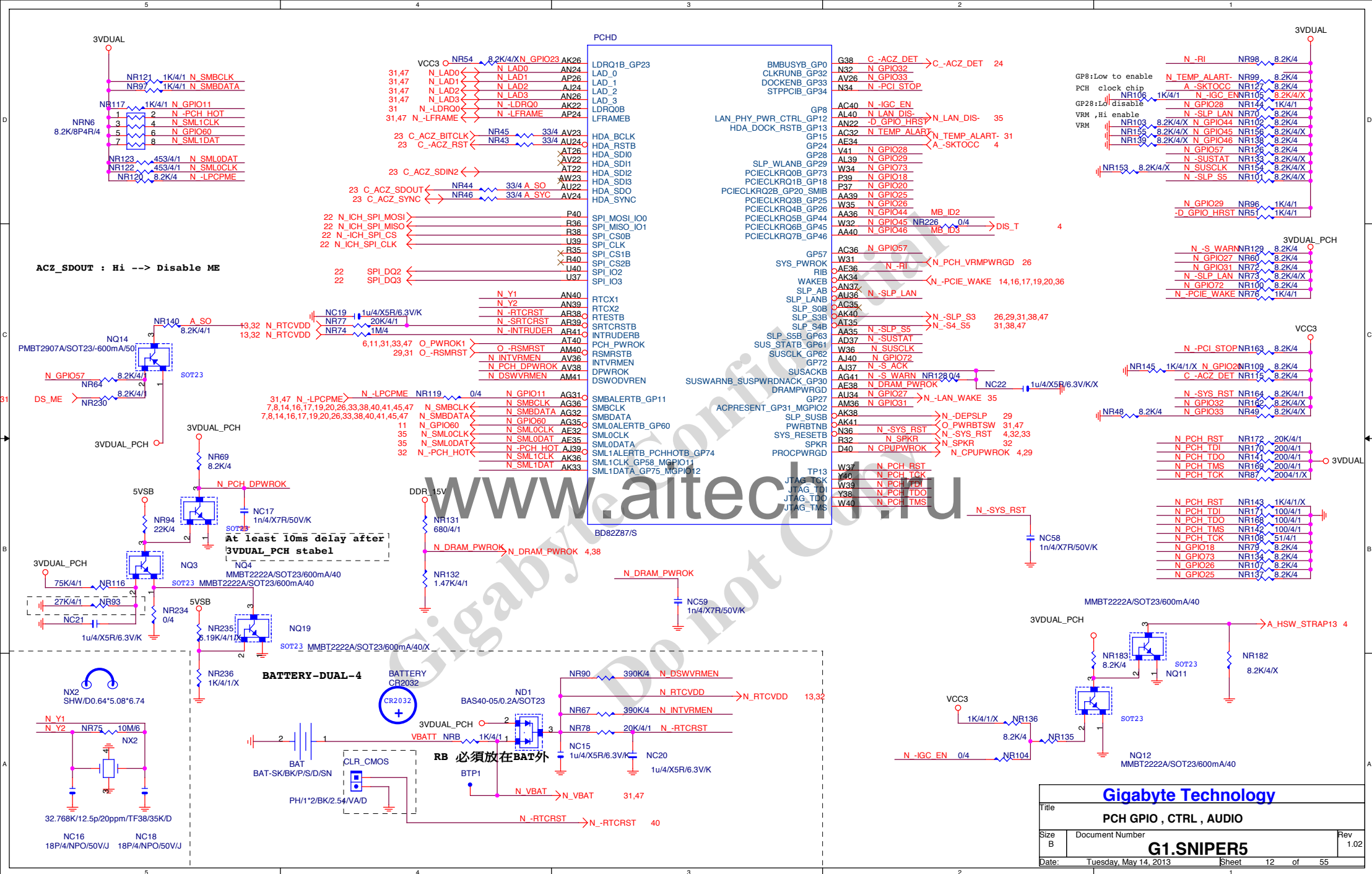


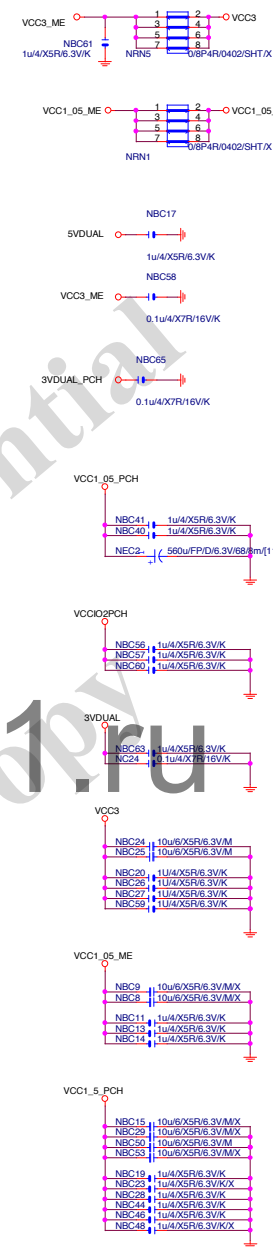
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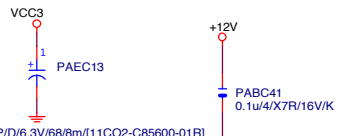
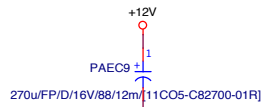
Gigabyte Technology

Title			
PCH FDI,DMI,USB,PCIe,NVRAM			
Size	Document Number	Rev	
Custom	G1.SNIPER5	1.02	
Date:	Tuesday, May 14, 2013	Sheet	9 of 55





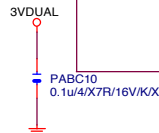
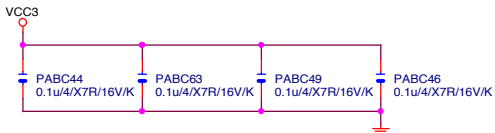




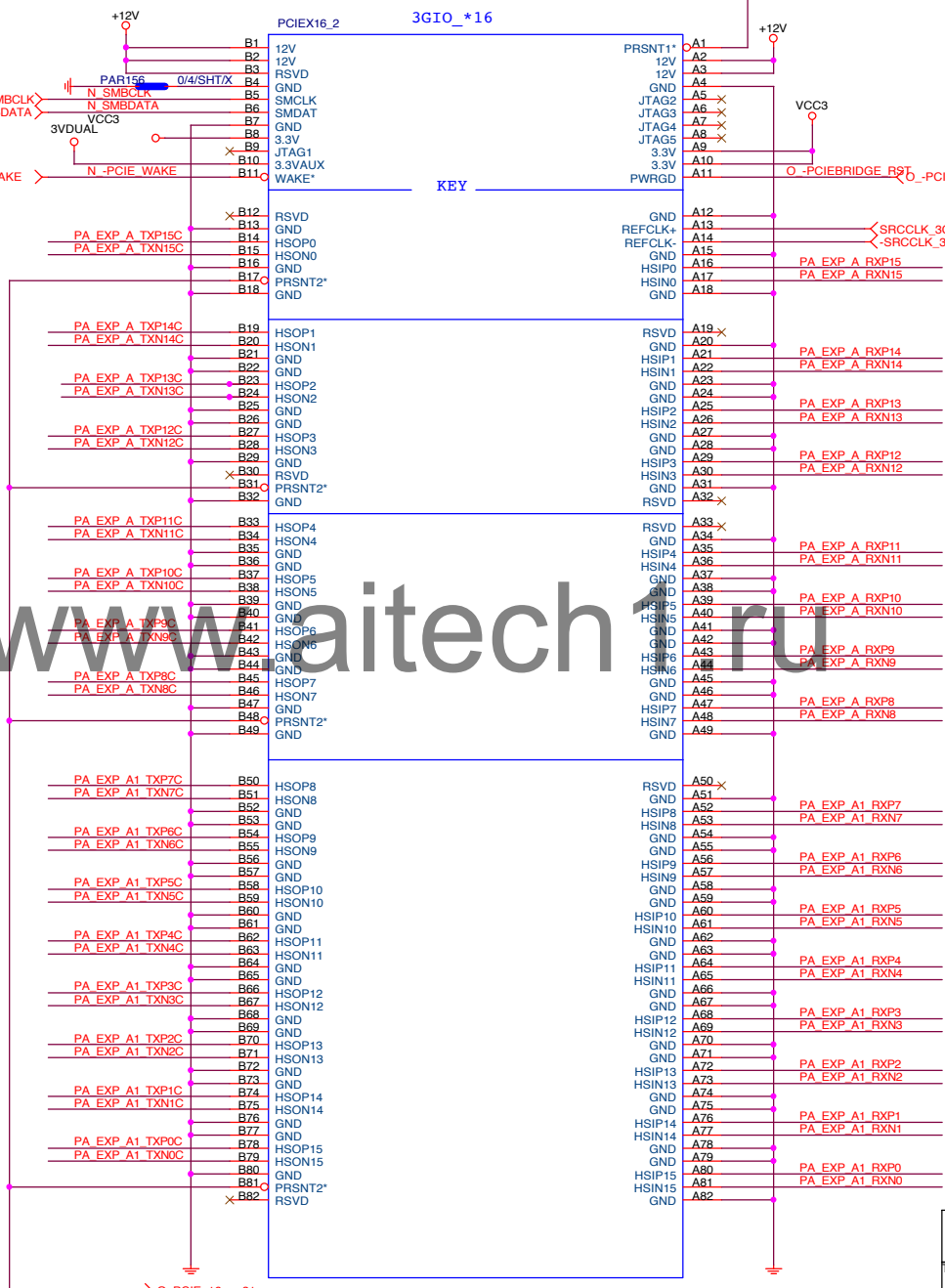
PCIESLOT-164DN-2

PA EXP A TXP15	PAC114	0.22u/4/X5R/6.3V/K	PA EXP A TXP15C
PA EXP A TXN15	PAC115	0.22u/4/X5R/6.3V/K	PA EXP A TXN15C
PA EXP A TXP14	PAC110	0.22u/4/X5R/6.3V/K	PA EXP A TXP14C
PA EXP A TXN14	PAC111	0.22u/4/X5R/6.3V/K	PA EXP A TXN14C
PA EXP A TXP13	PAC109	0.22u/4/X5R/6.3V/K	PA EXP A TXP13C
PA EXP A TXN13	PAC107	0.22u/4/X5R/6.3V/K	PA EXP A TXN13C
PA EXP A TXP12	PAC108	0.22u/4/X5R/6.3V/K	PA EXP A TXP12C
PA EXP A TXN12	PAC106	0.22u/4/X5R/6.3V/K	PA EXP A TXN12C
PA EXP A TXP11	PAC97	0.22u/4/X5R/6.3V/K	PA EXP A TXP11C
PA EXP A TXN11	PAC99	0.22u/4/X5R/6.3V/K	PA EXP A TXN11C
PA EXP A TXP10	PAC92	0.22u/4/X5R/6.3V/K	PA EXP A TXP10C
PA EXP A TXN10	PAC93	0.22u/4/X5R/6.3V/K	PA EXP A TXN10C
PA EXP A TXP9	PAC87	0.22u/4/X5R/6.3V/K	PA EXP A TXP9C
PA EXP A TXN9	PAC88	0.22u/4/X5R/6.3V/K	PA EXP A TXN9C
PA EXP A TXP8	PAC83	0.22u/4/X5R/6.3V/K	PA EXP A TXP8C
PA EXP A TXN8	PAC85	0.22u/4/X5R/6.3V/K	PA EXP A TXN8C
PA EXP A1 TXP7	PAC80	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP7C
PA EXP A1 TXN7	PAC82	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN7C
PA EXP A1 TXP6	PAC74	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP6C
PA EXP A1 TXN6	PAC77	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN6C
PA EXP A1 TXP5	PAC68	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP5C
PA EXP A1 TXN5	PAC70	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN5C
PA EXP A1 TXP4	PAC62	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP4C
PA EXP A1 TXN4	PAC64	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN4C
PA EXP A1 TXP3	PAC56	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP3C
PA EXP A1 TXN3	PAC58	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN3C
PA EXP A1 TXP2	PAC50	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP2C
PA EXP A1 TXN2	PAC52	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN2C
PA EXP A1 TXP1	PAC43	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP1C
PA EXP A1 TXN1	PAC46	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN1C
PA EXP A1 TXP0	PAC39	0.22u/4/X5R/6.3V/K	PA EXP A1 TXP0C
PA EXP A1 TXN0	PAC38	0.22u/4/X5R/6.3V/K	PA EXP A1 TXN0C

PA EXP A1 RXP18..15]	>>>PA_EXP_A_RXP[8..15]	42
PA EXP A1 RXN18..15]	>>>PA_EXP_A_RXN[8..15]	42
PA EXP A1 TXP18..15]	>>>PA_EXP_A_TXP[8..15]	42
PA EXP A1 TXN18..15]	>>>PA_EXP_A_TXN[8..15]	42
PA EXP A1 RXP10..7]	>>>PA_EXP_A1_RXP[0..7]	15
PA EXP A1 RXN10..7]	>>>PA_EXP_A1_RXN[0..7]	15
PA EXP A1 TXP10..7]	>>>PA_EXP_A1_TXP[0..7]	15
PA EXP A1 TXN10..7]	>>>PA_EXP_A1_TXN[0..7]	15



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Title

PCI EXPRESS X16 PORT_1

Size

Document Number

G1.SNIPERS5

Rev

1.02

Date:

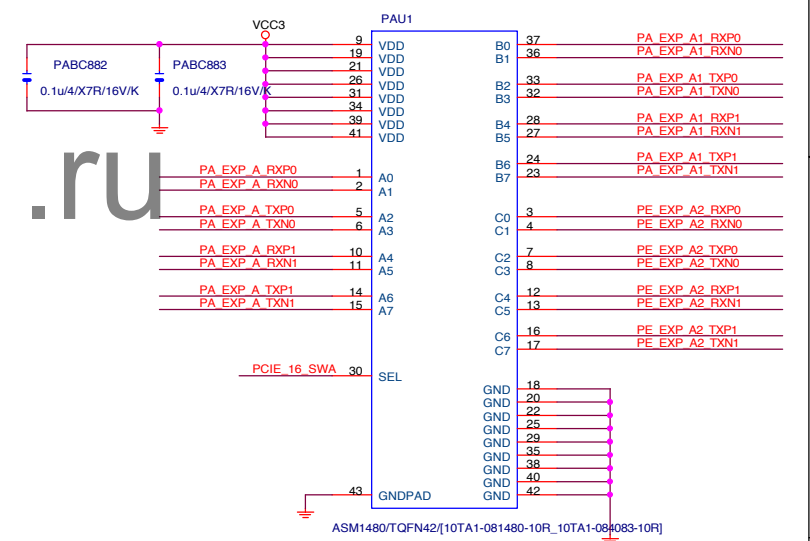
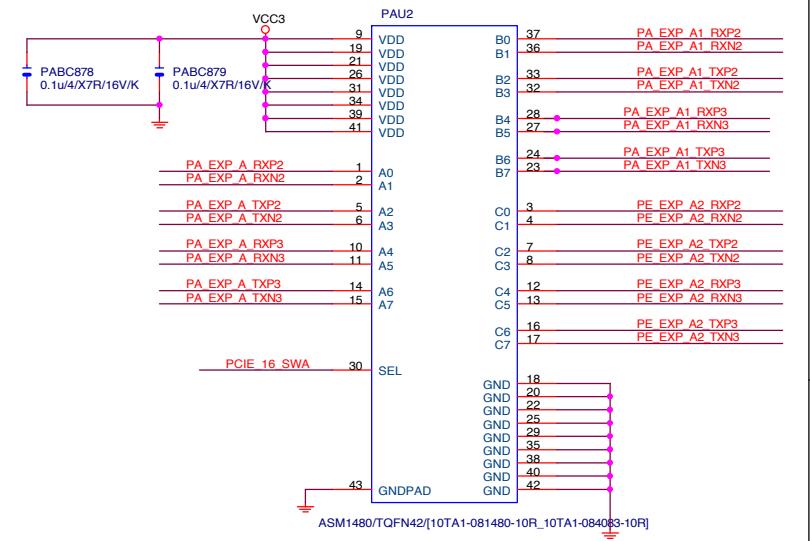
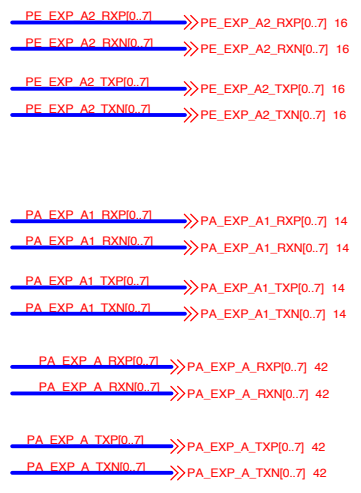
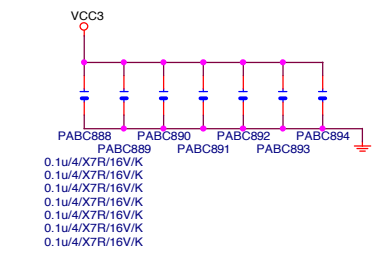
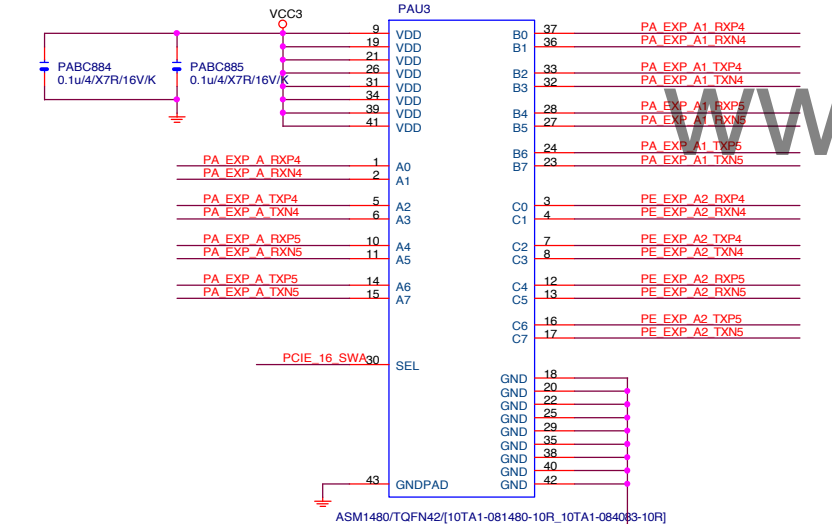
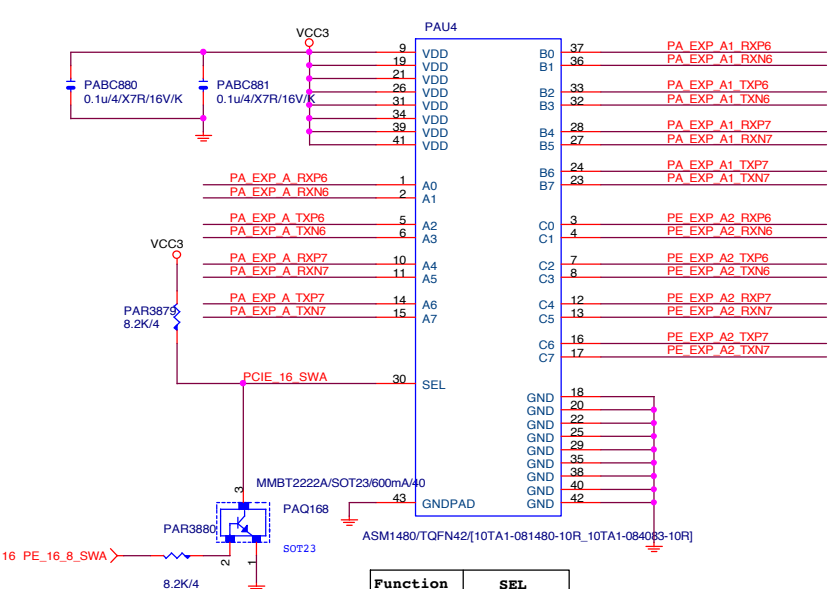
Tuesday, May 14, 2013

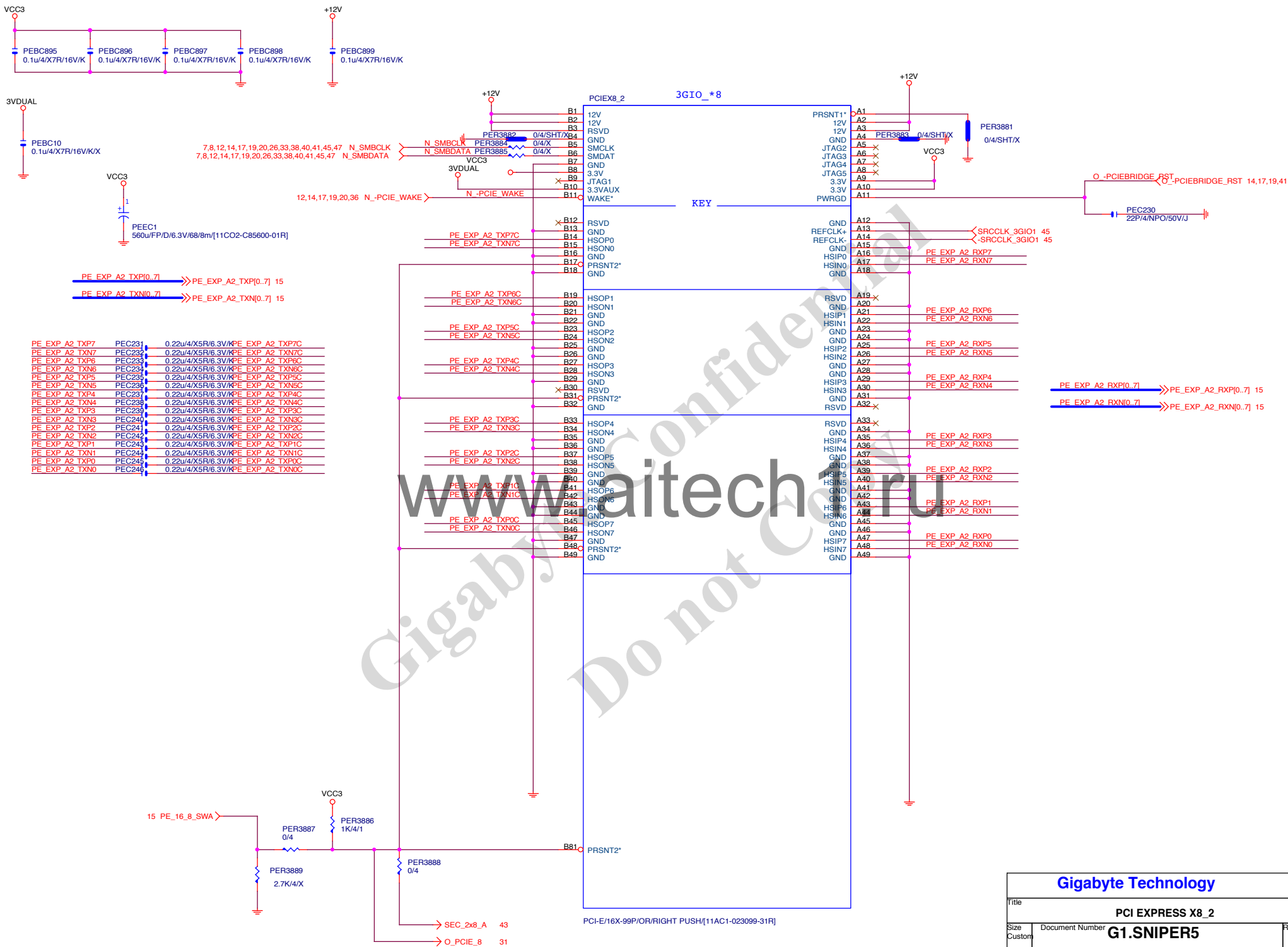
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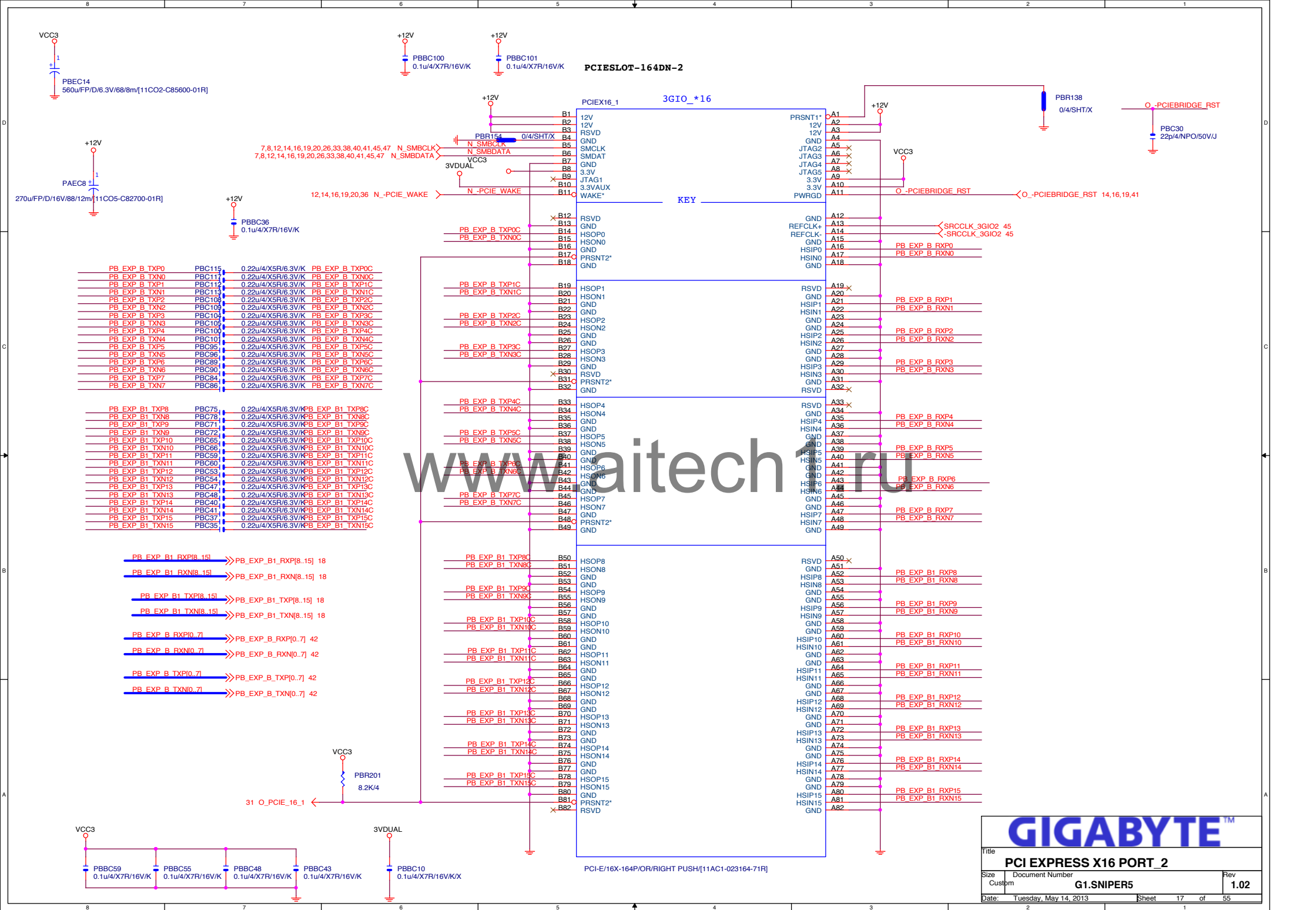
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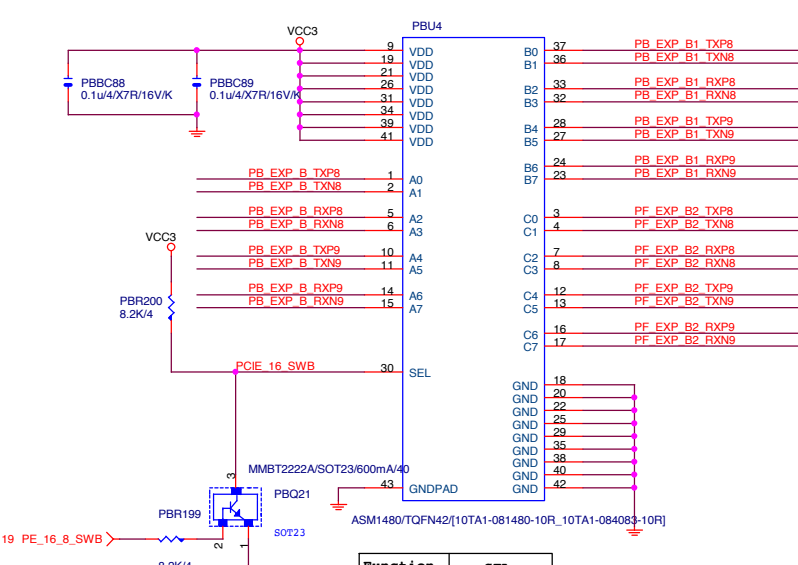
of

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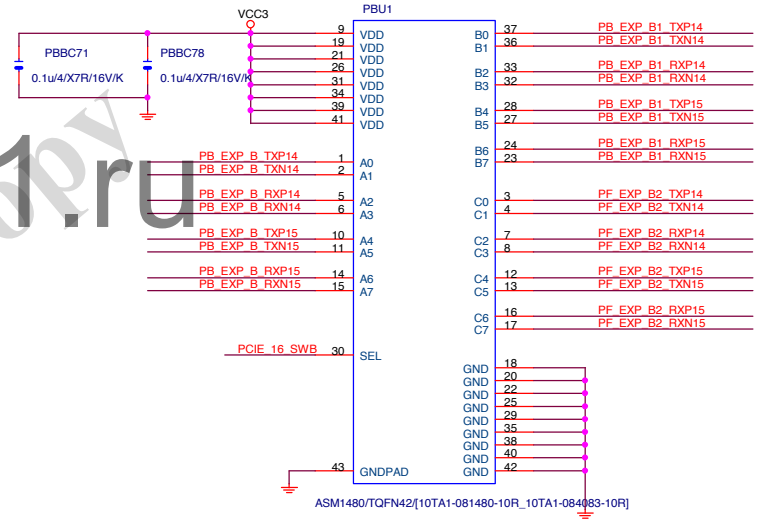
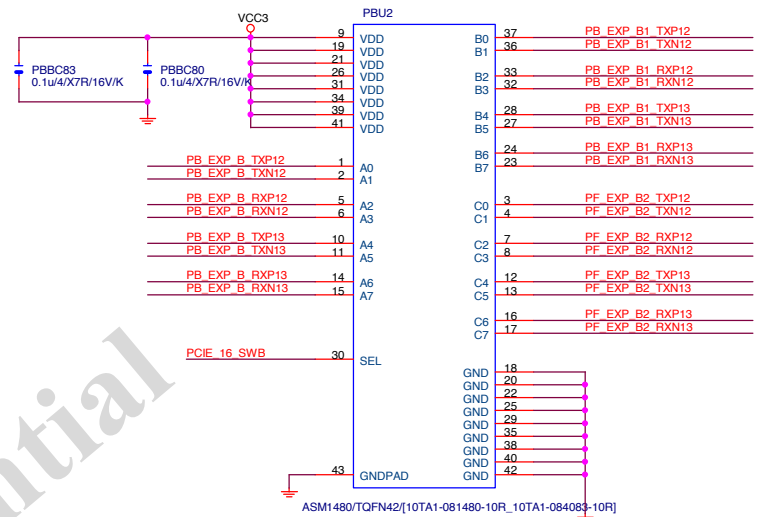
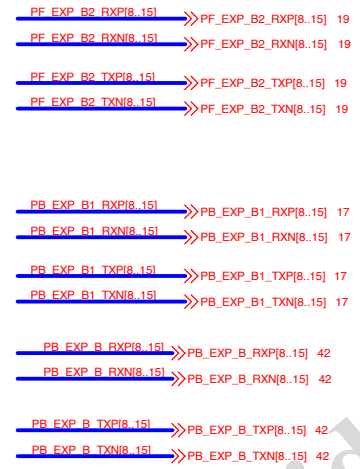
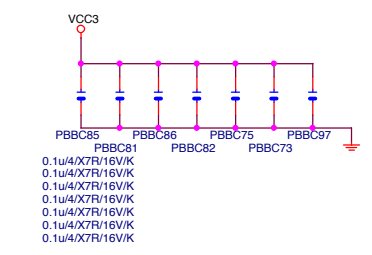
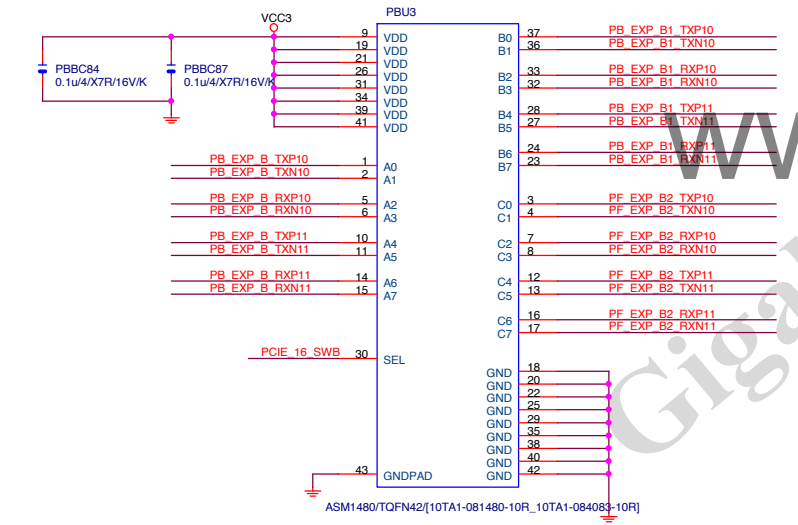








Function	SEL
A--> B	L
A--> C	H



Title

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Custom

Date:

PCI EXPRESS X16 SWITCH_2

G1.SNIPER5

Tuesday, May 14, 2013

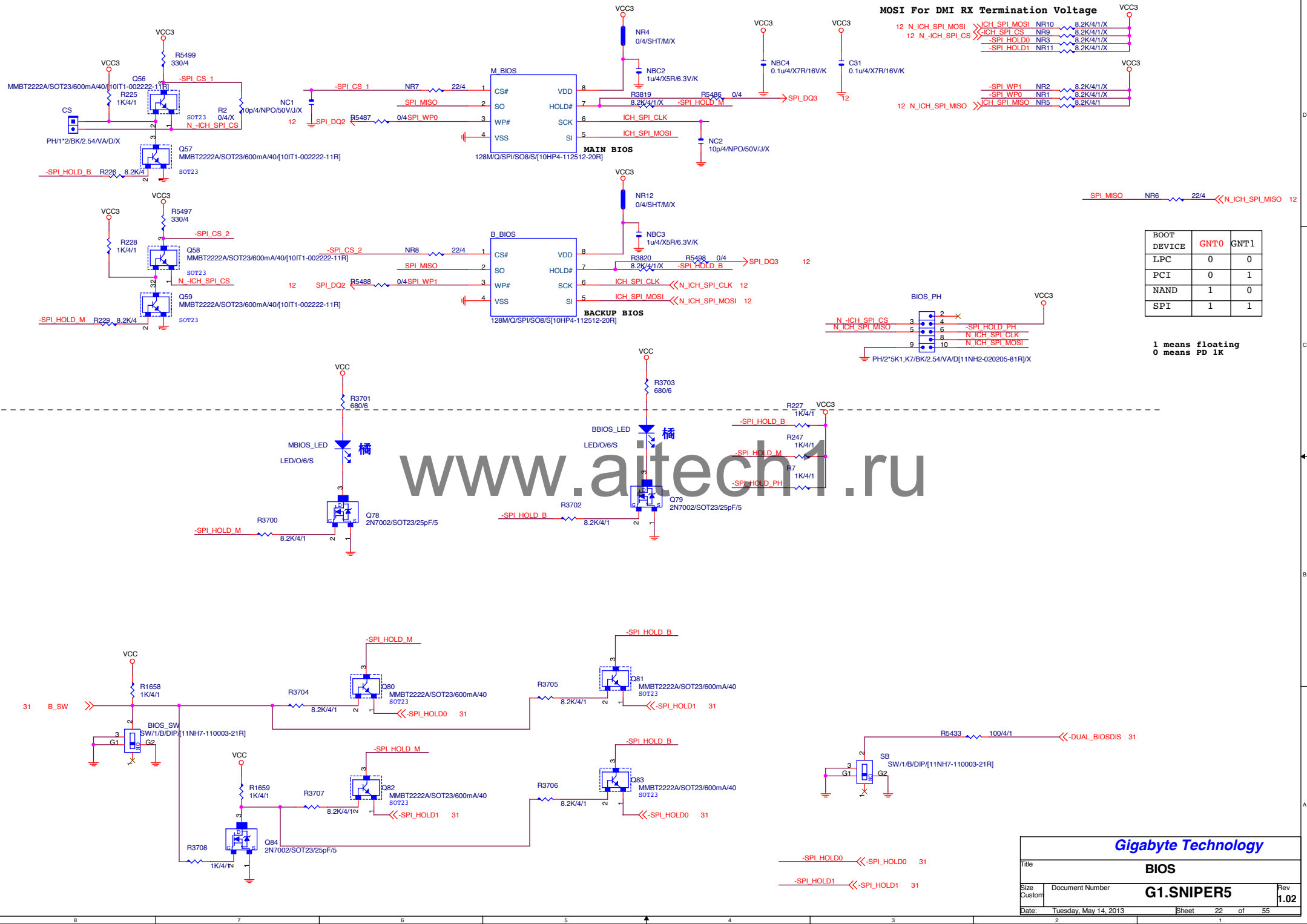
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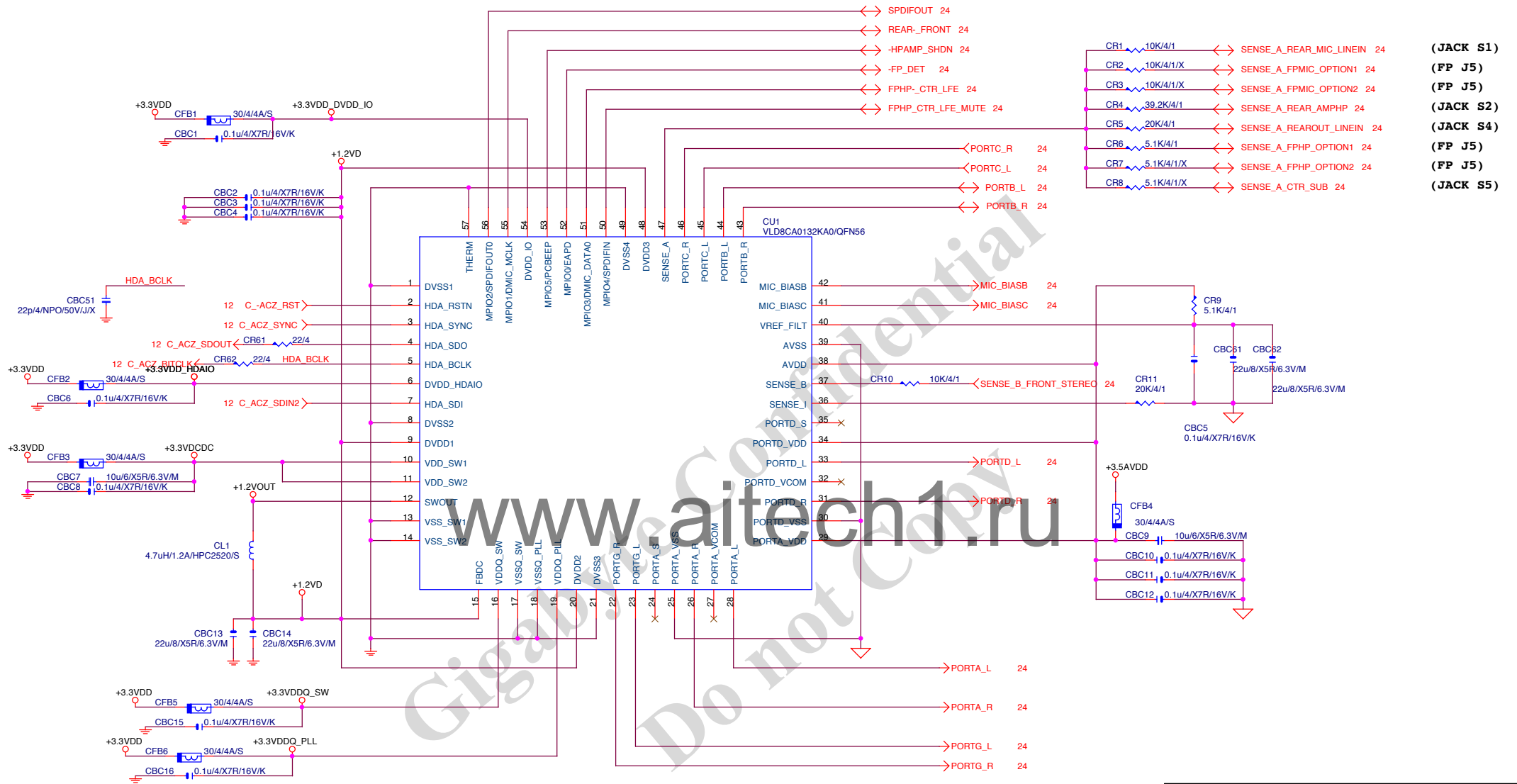
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18 of 55

Rev

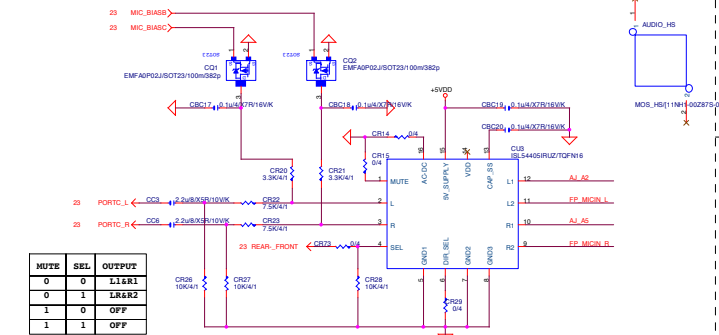
1.02



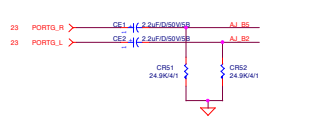


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Title			
MALCOLM-EX			
Size	Document Number	Rev	
Custom	G1.SNIPER5	1.02	
Date:	Tuesday, May 14, 2013	Sheet	23 of 55

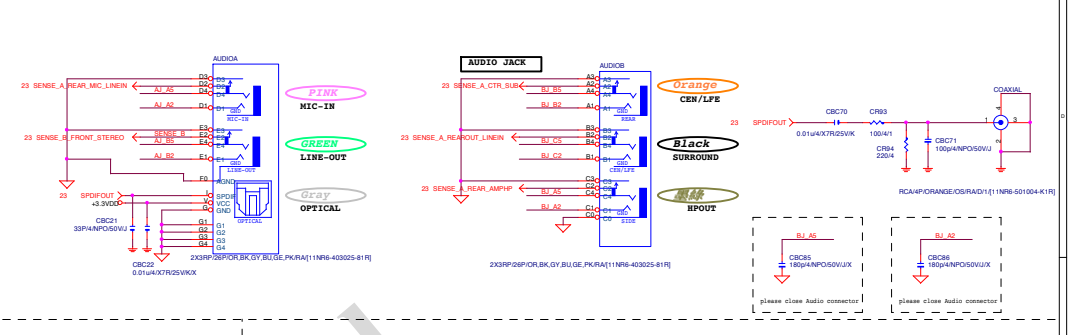
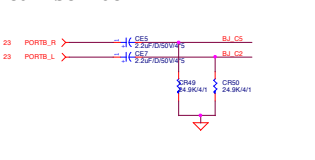
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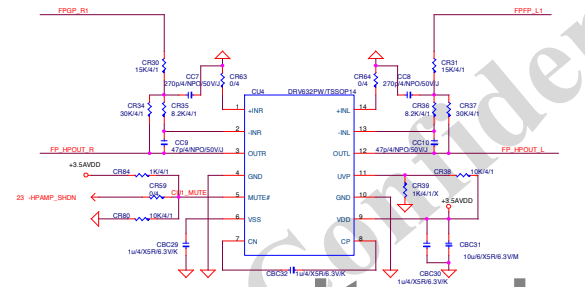
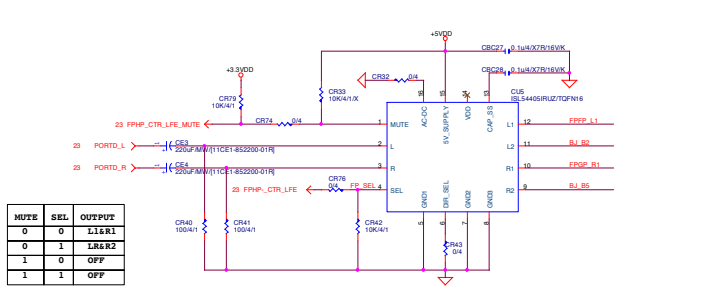
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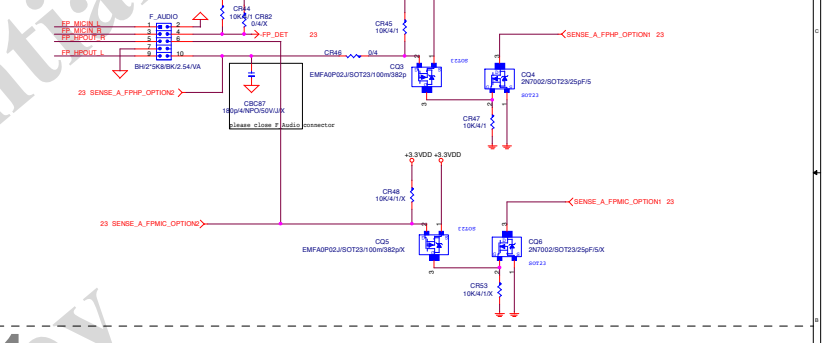
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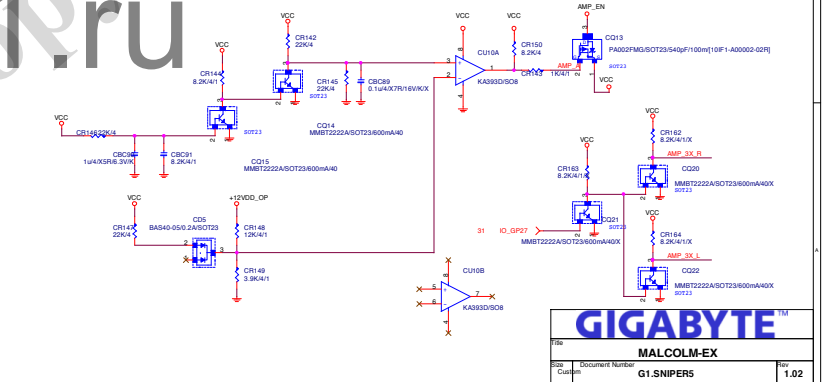
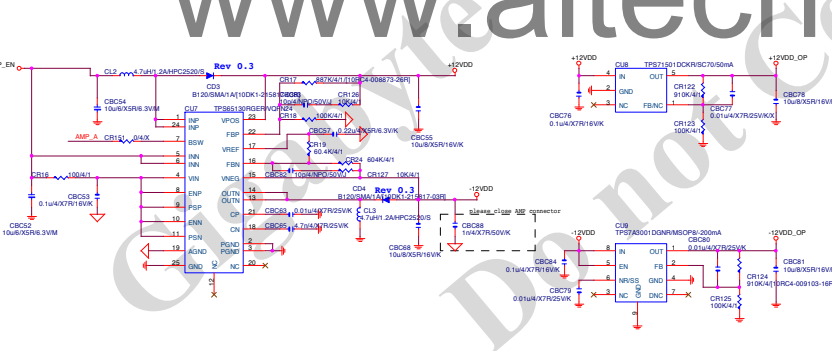
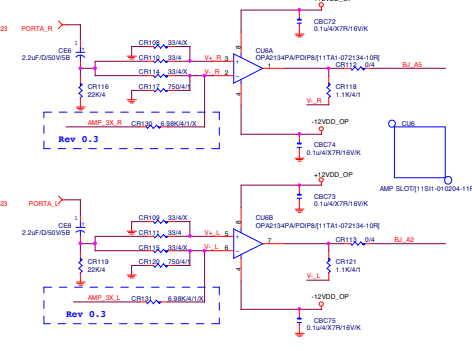
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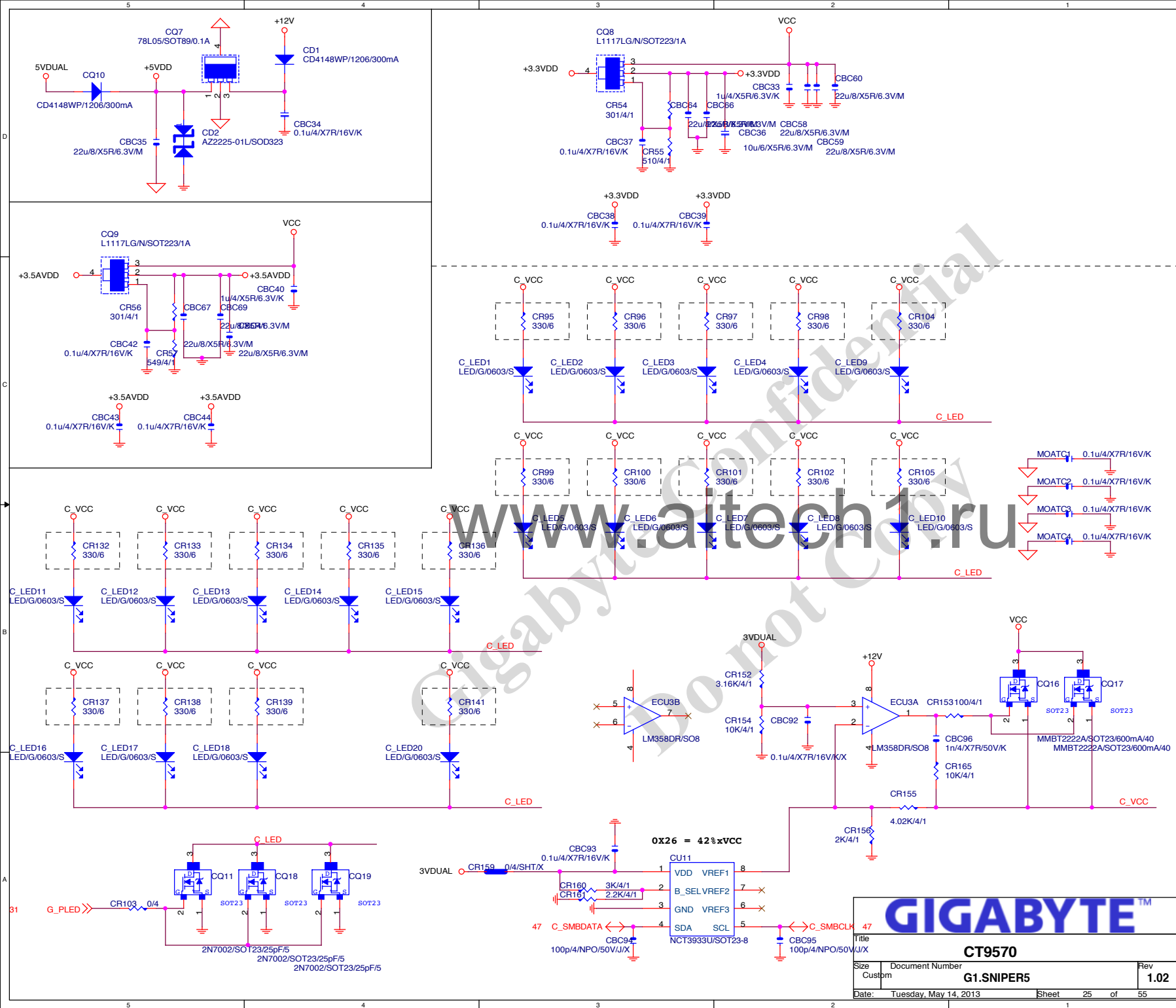
HD Audio FRONT PANEL



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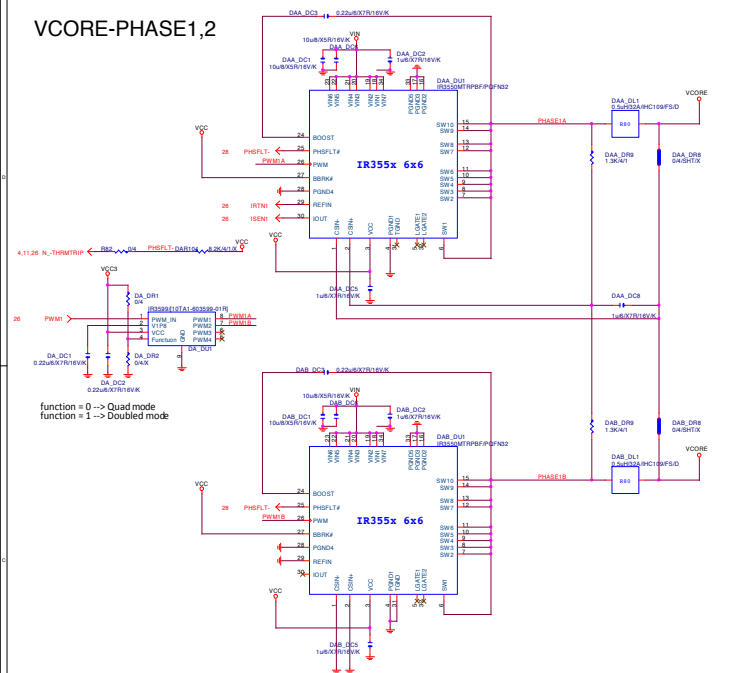


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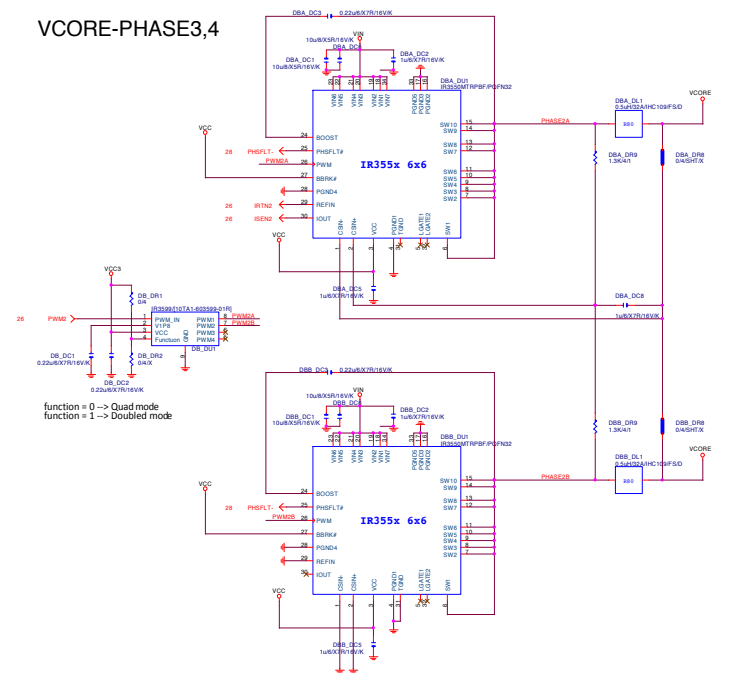
CT9570

Title	Document Number	Rev
Size	Custom	1.02
Date:	Tuesday, May 14, 2013	Sheet 25 of 55

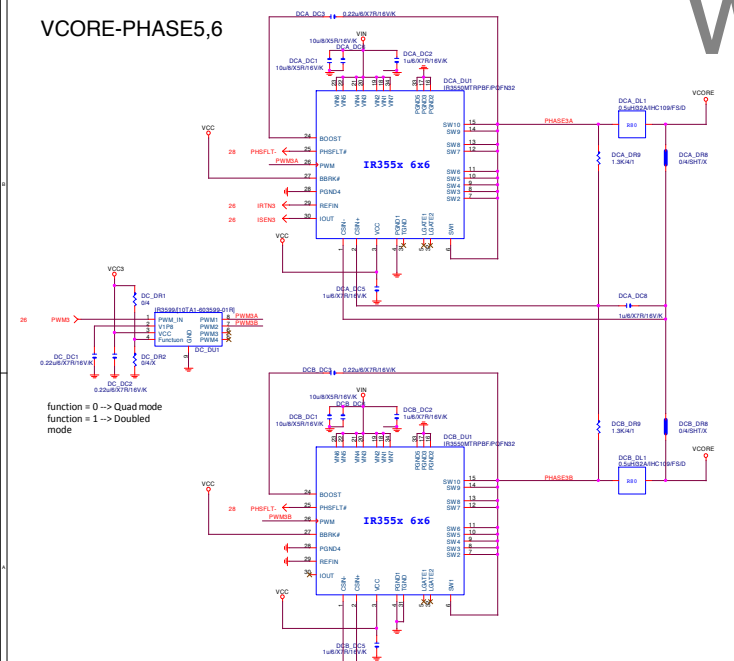
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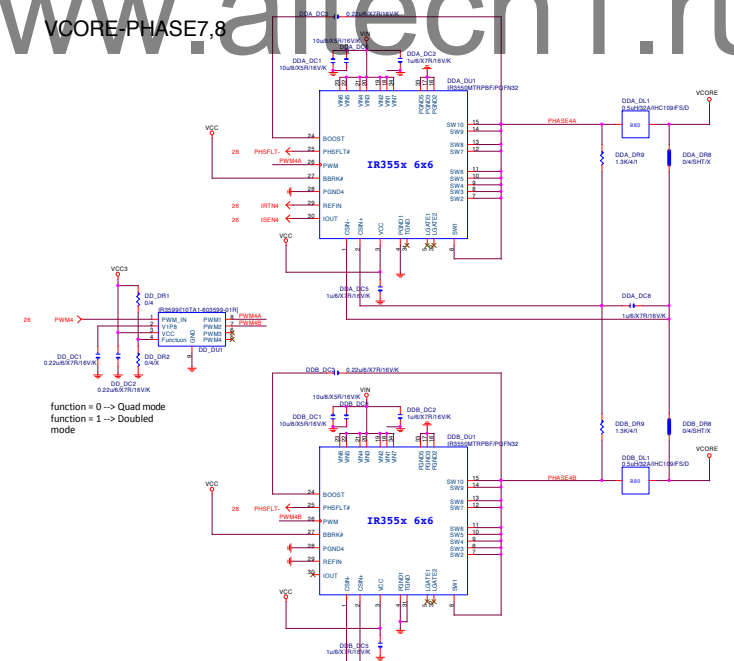
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VCORE-PHASE5,6

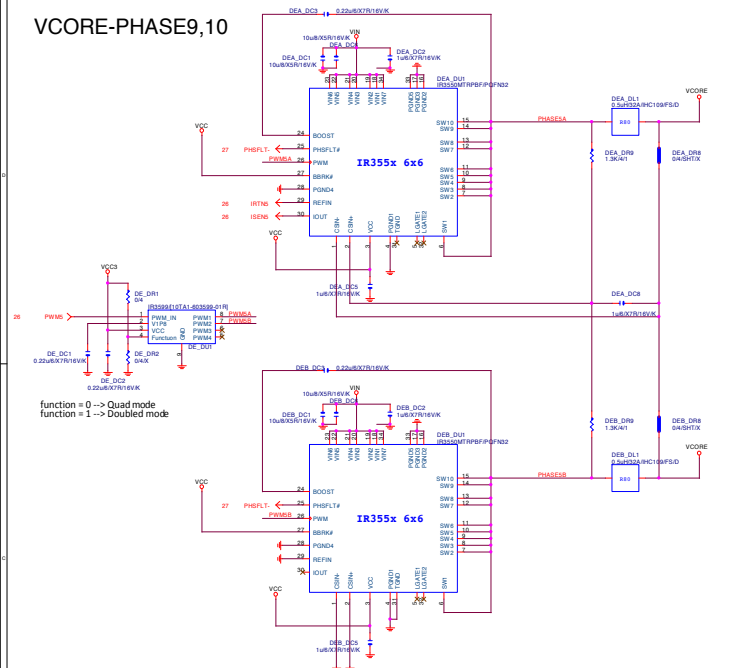


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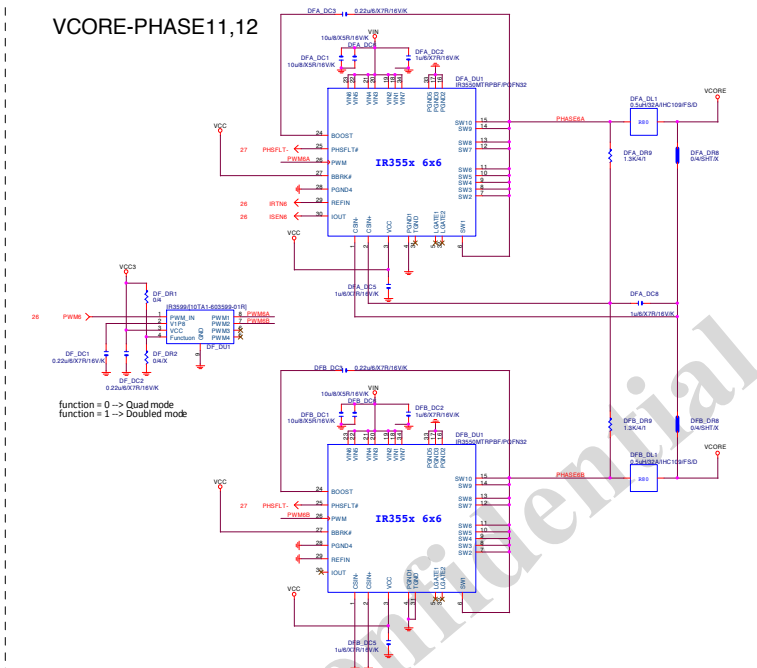


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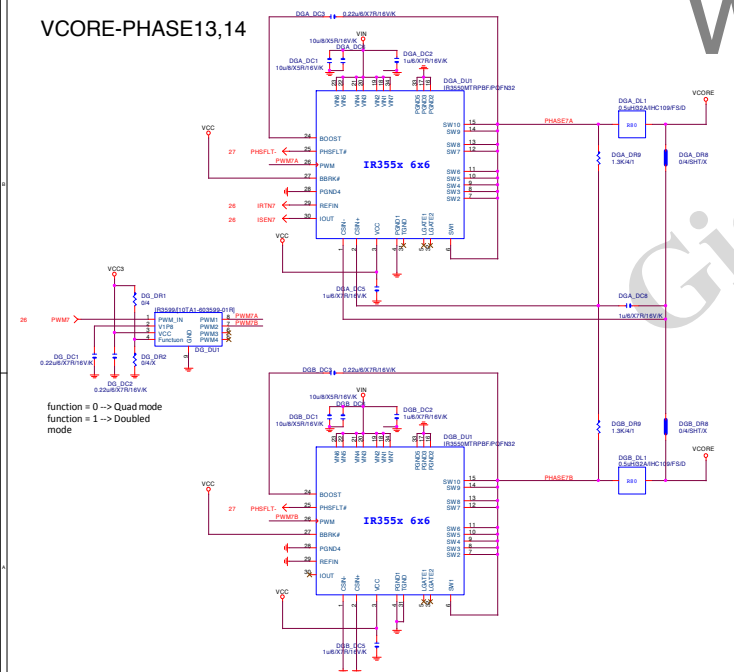
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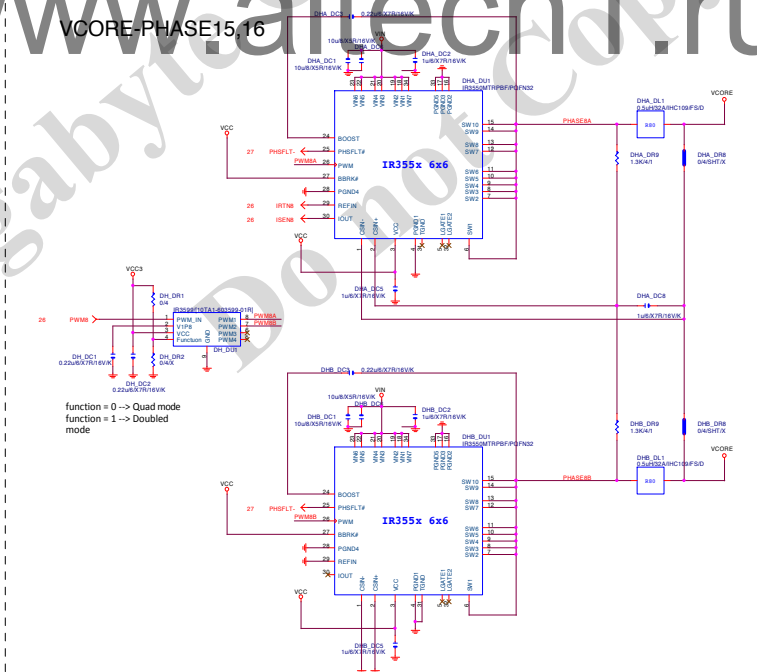
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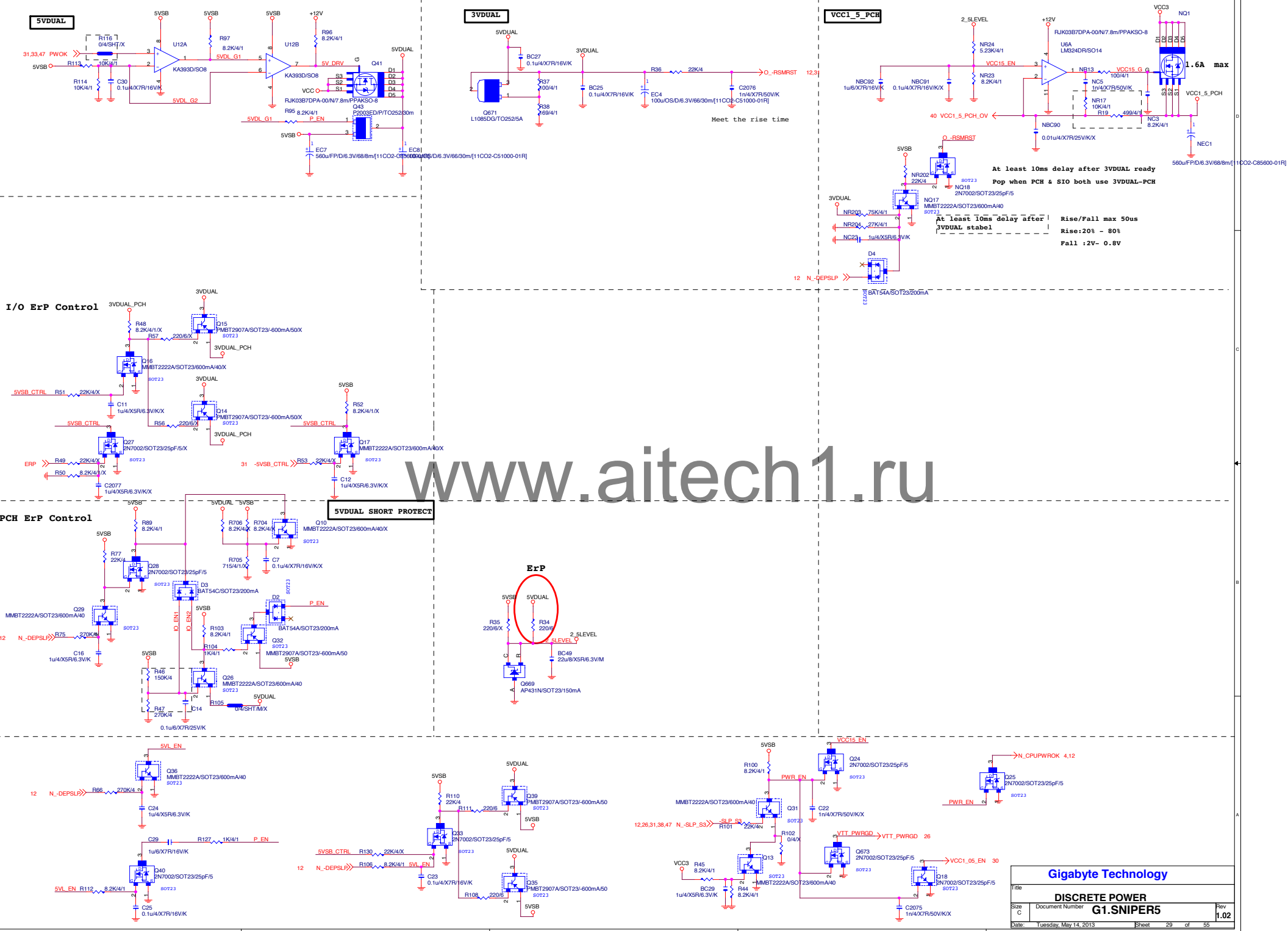


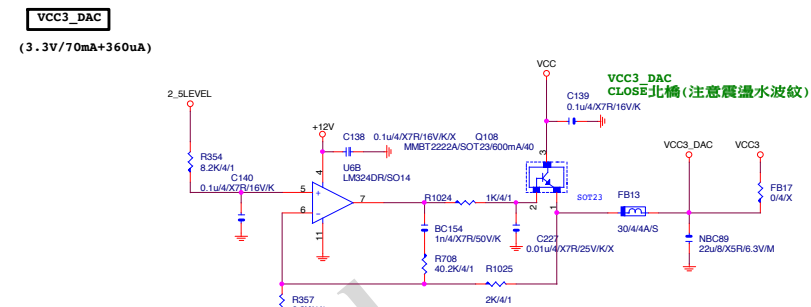
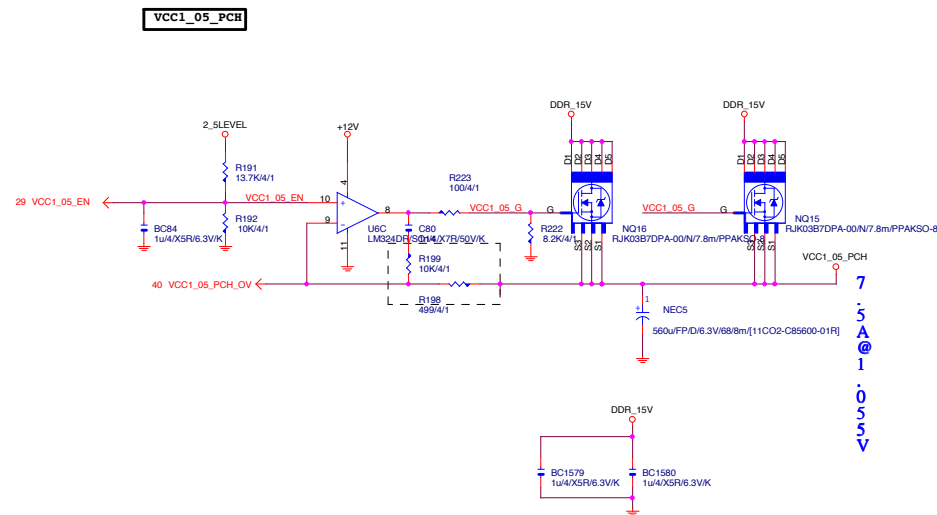
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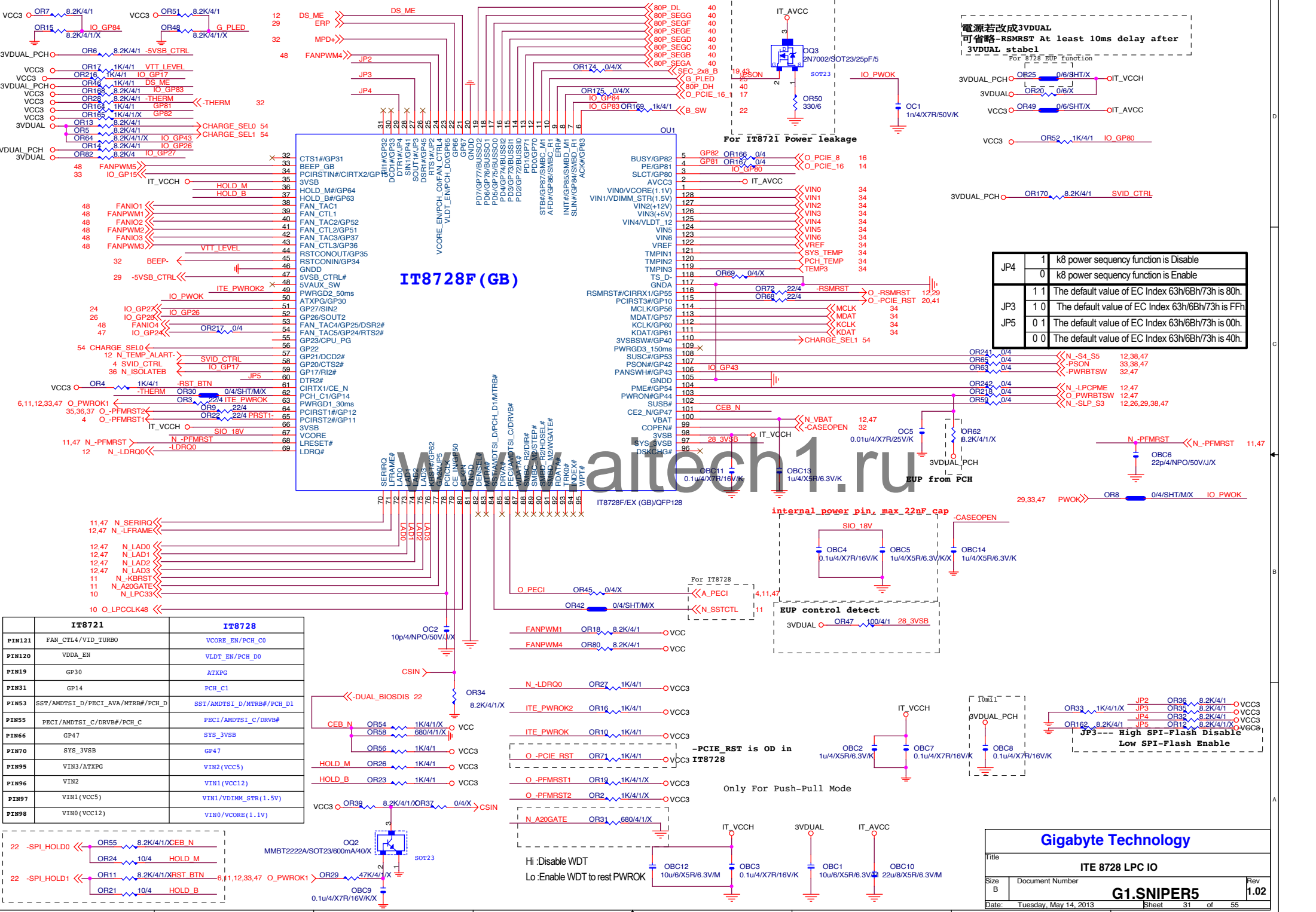
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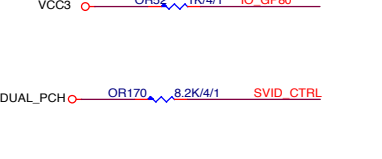
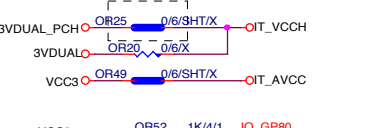




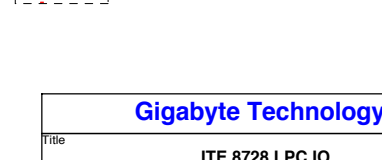
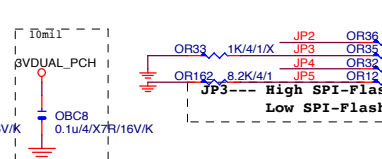
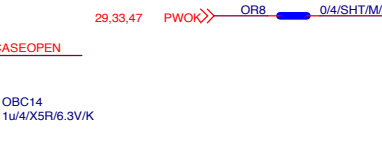
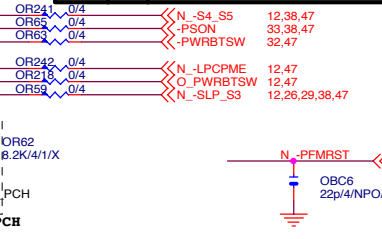
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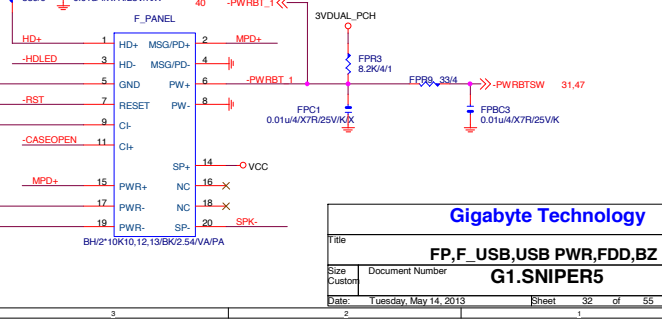
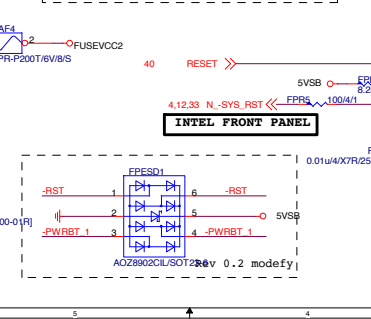
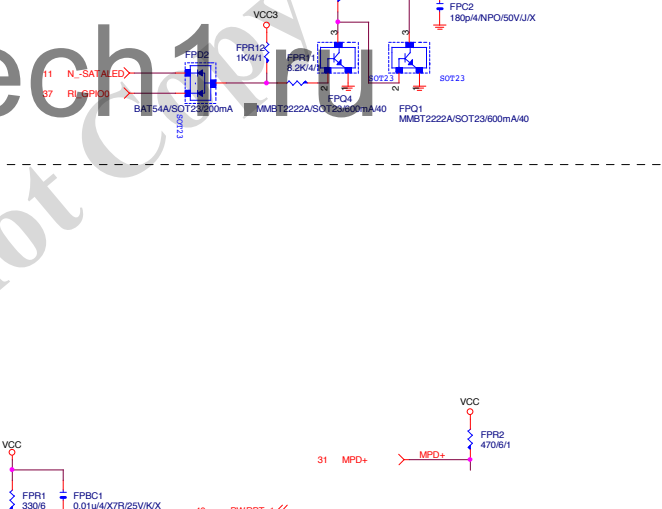
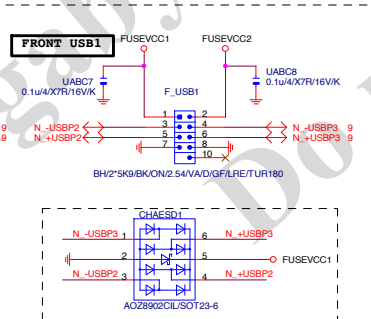
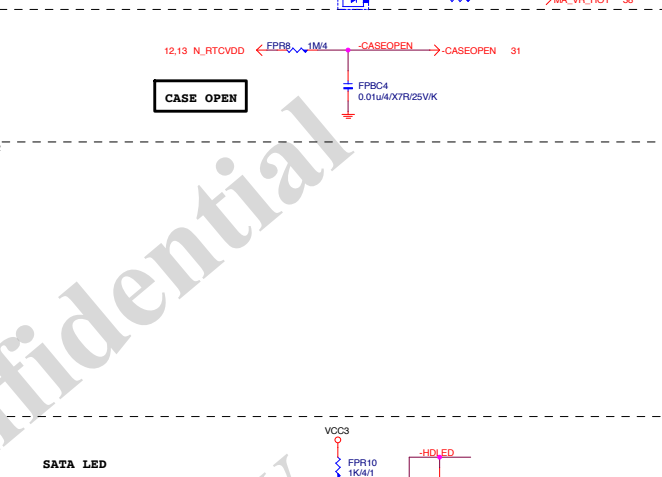
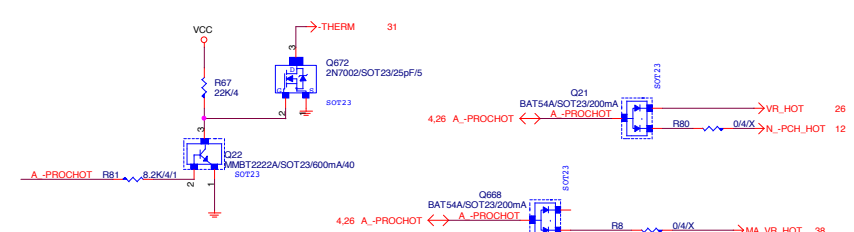
電源若改成3VDUAL
可省略-RSMRST At least 10ms delay after
3VDUAL stabel
For 8728 EUP Function



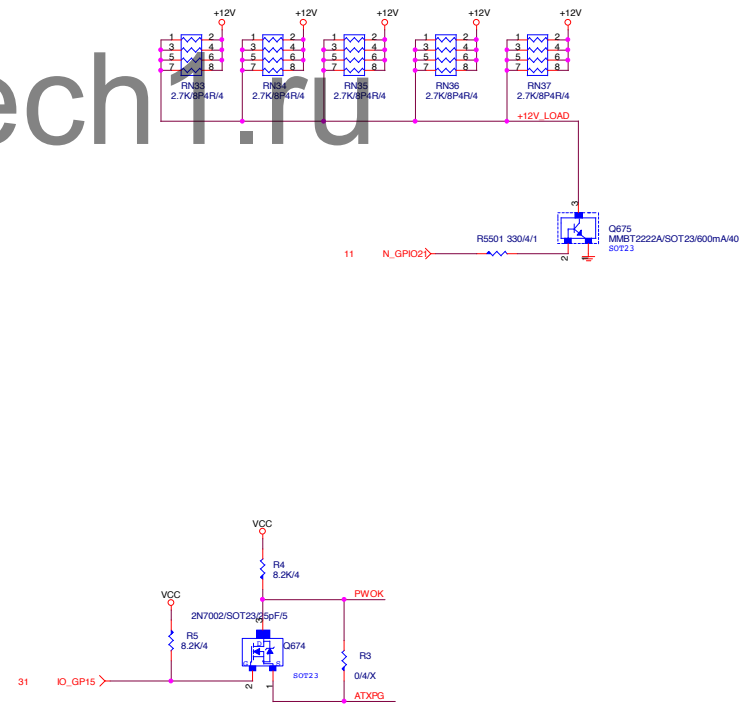
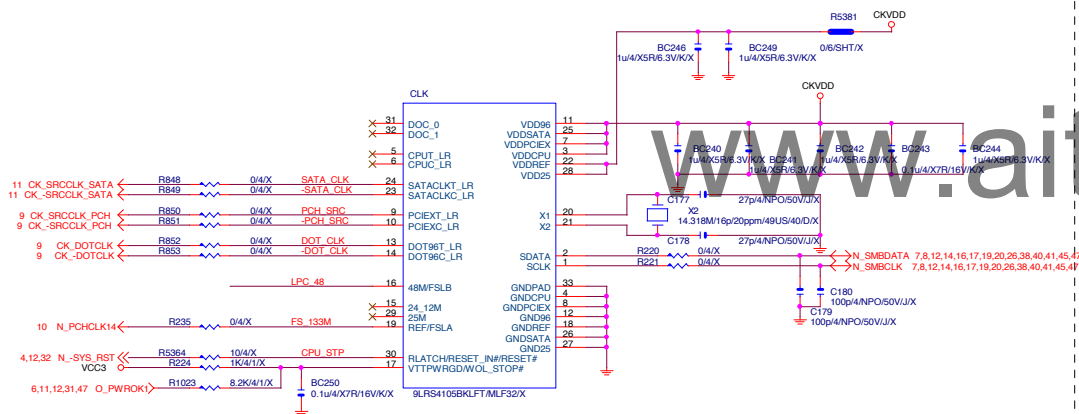
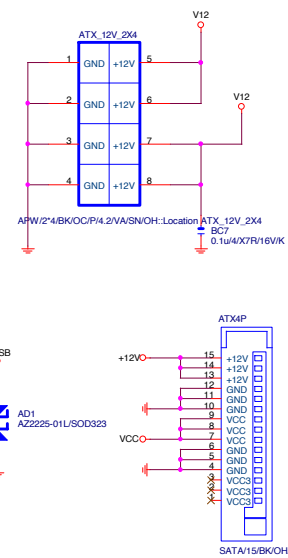
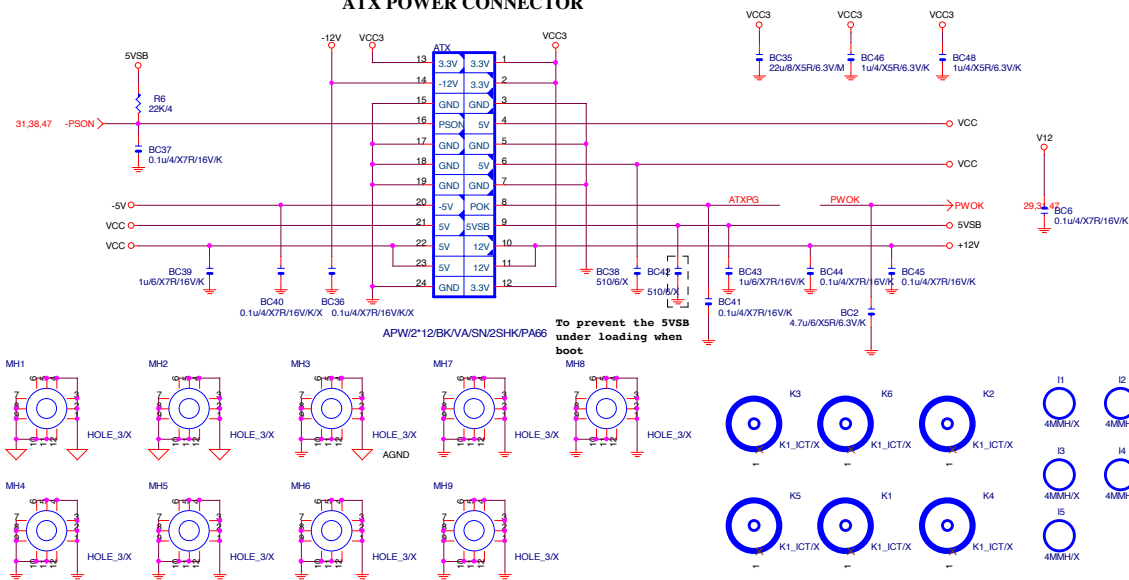
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.



Gigabyte Technology			
Title			
ITE 8728 LPC IO			
Size	Document Number	Rev	
B		G1.SNIPER5	
Date:	Tuesday, May 14, 2013	Sheet	31 of 55



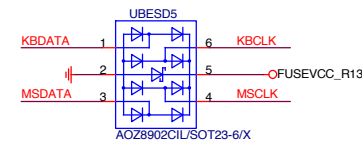
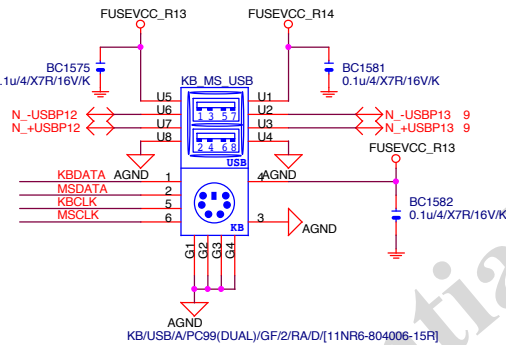
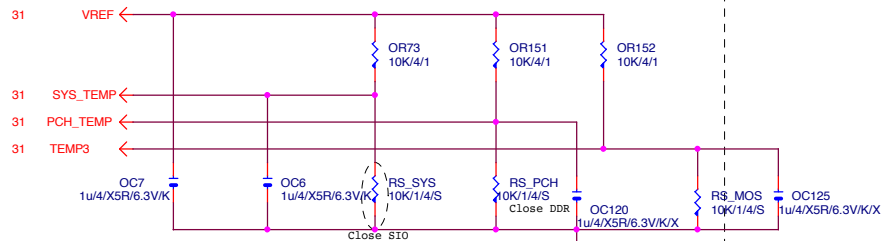
ATX POWER CONNECTOR

**CLK GEN CK505**

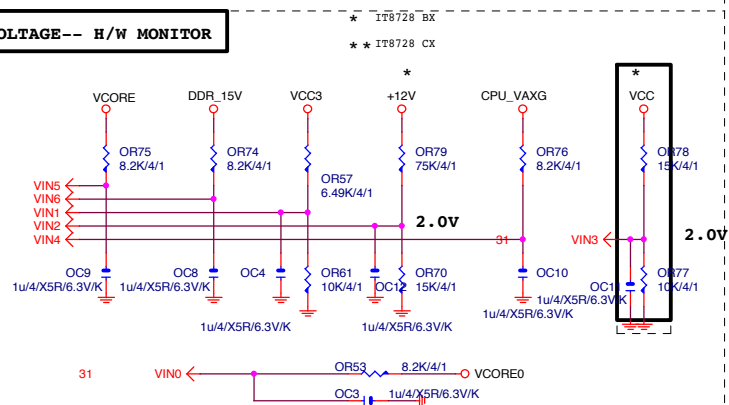
CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M

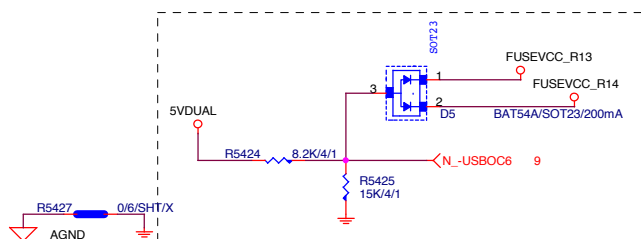
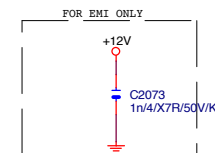
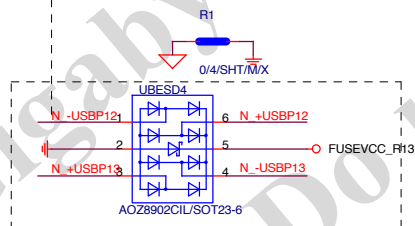
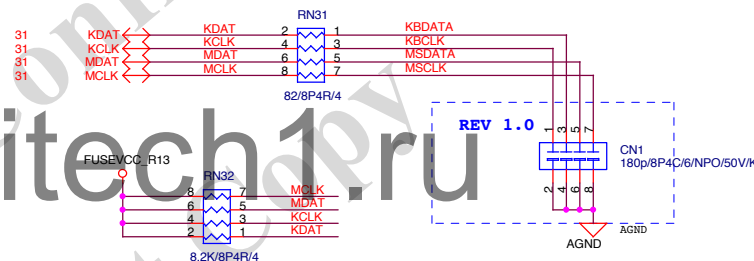
TEMP H/W MONITOR



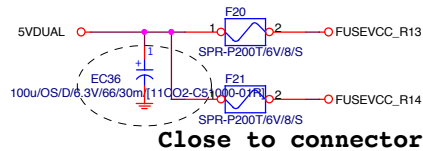
VOLTAGE-- H/W MONITOR



The division voltage of VIN2 & VIN3 must be around 2.0V
V-FOR E-VERSION

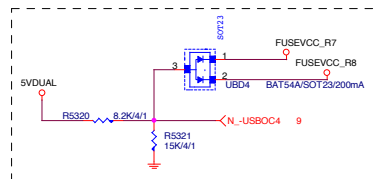
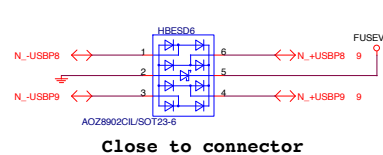
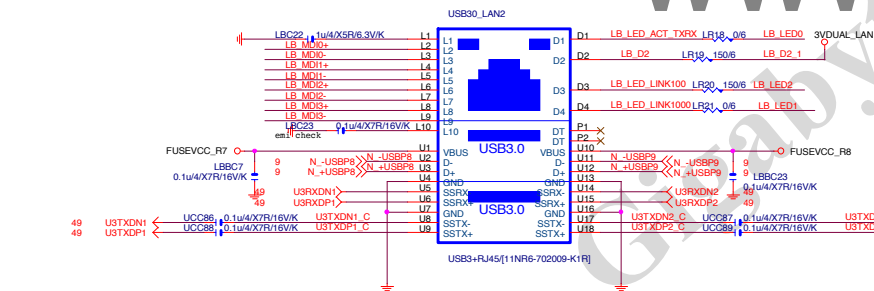
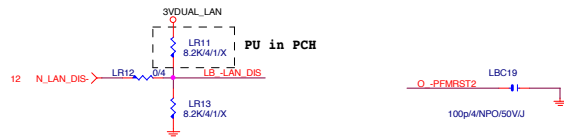
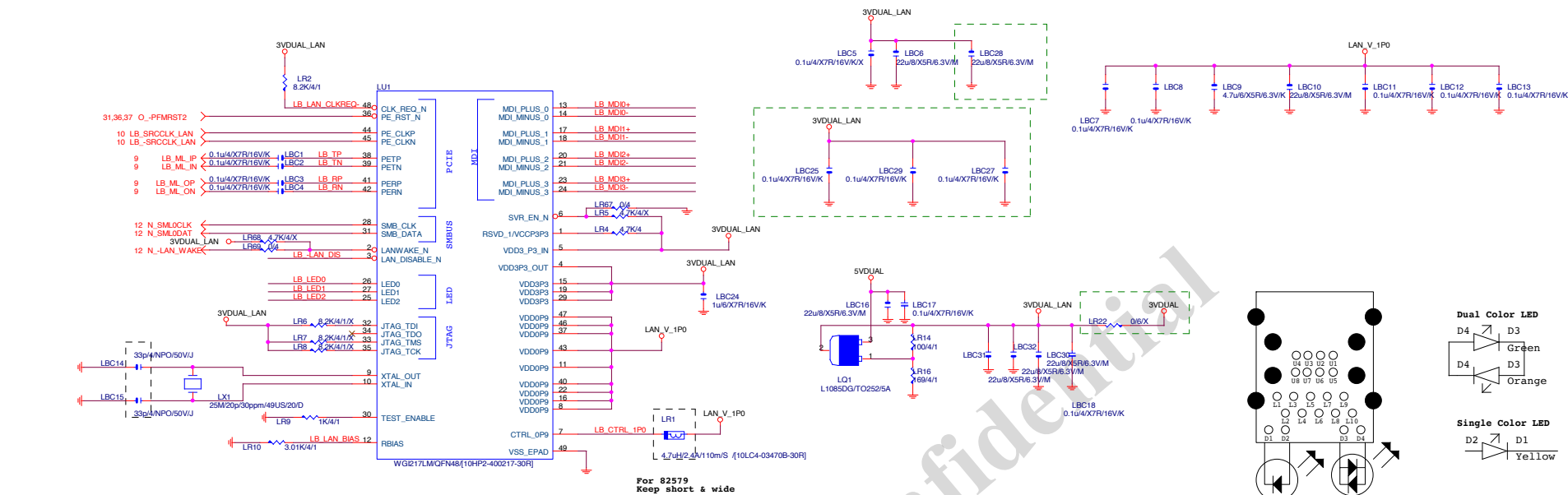


USB X3 POWER

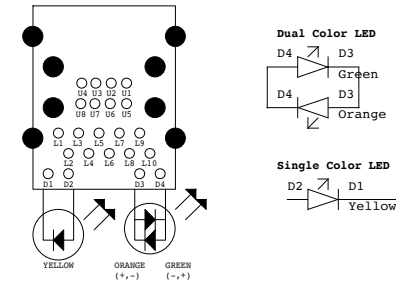


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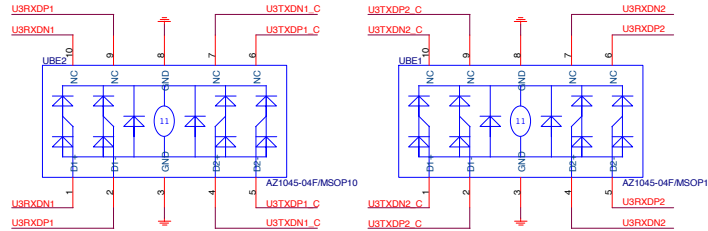
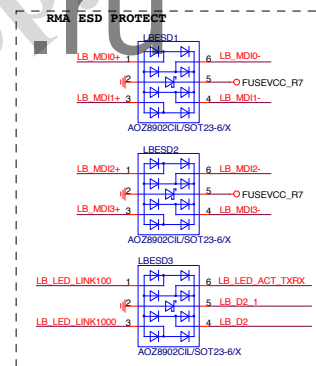
Title			HWM,KB/MS, FAN CTRL		
Size	Document Number	Rev			
Custom	G1.SNIPER5			1.02	
Date:	Tuesday, May 14, 2013	Sheet	34	of	55

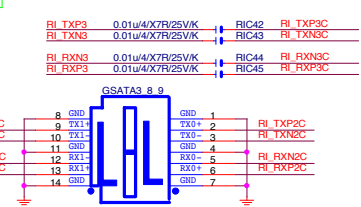
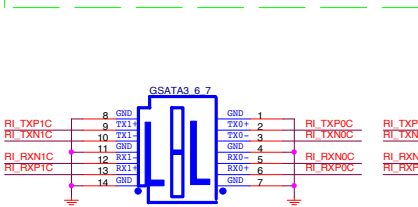
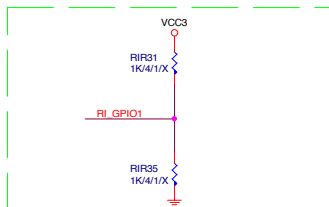
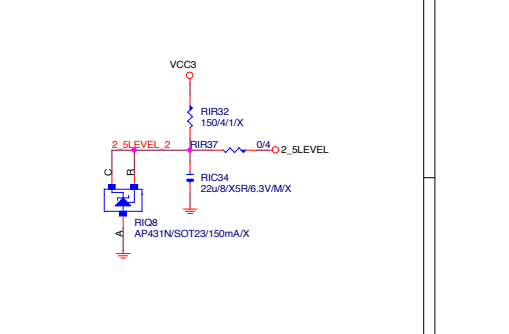
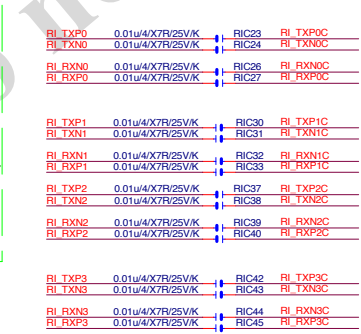
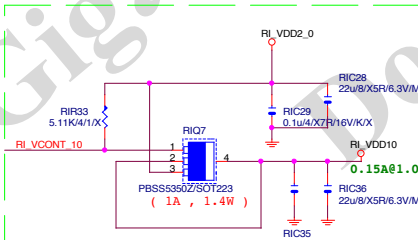
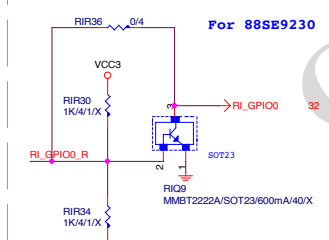
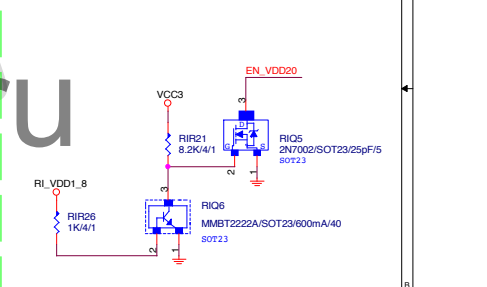
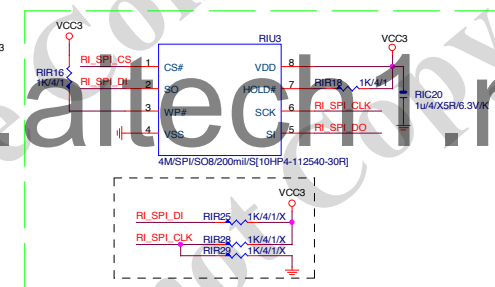
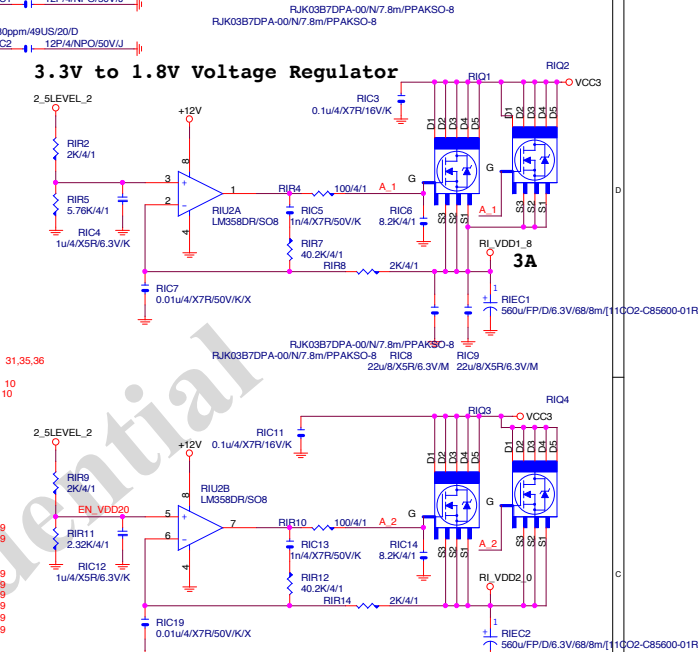
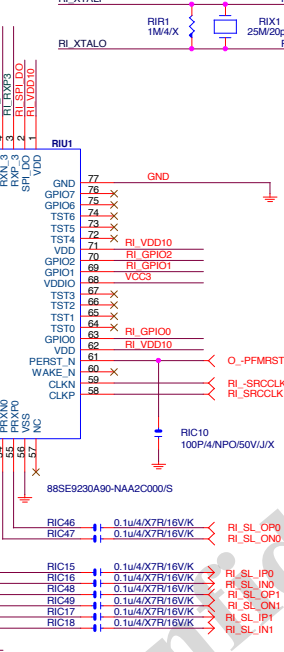
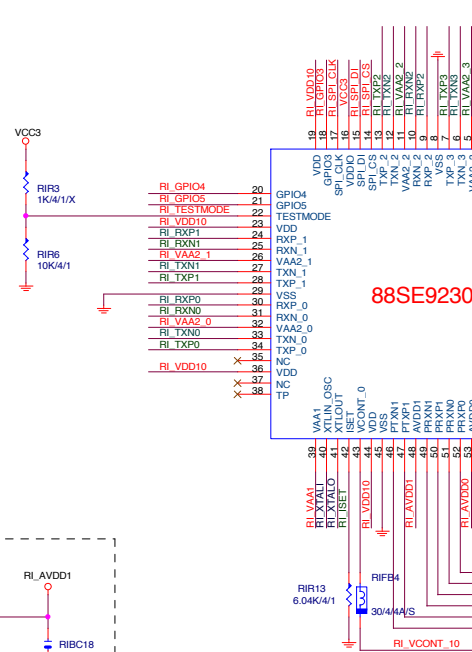
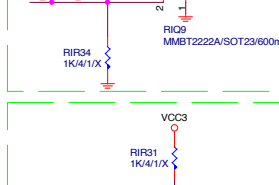
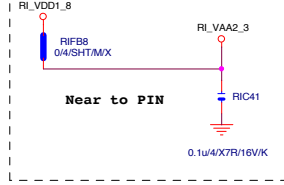
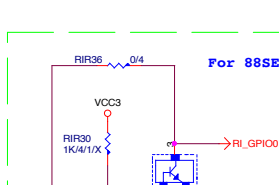
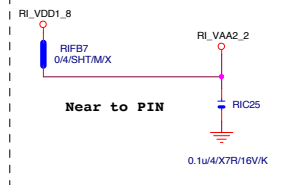
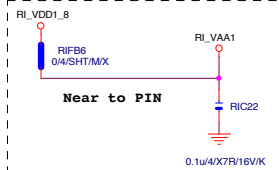
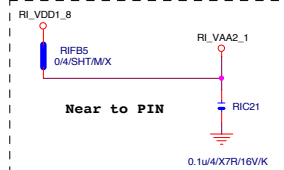
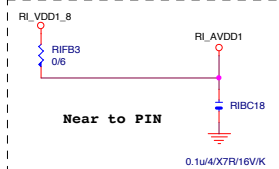
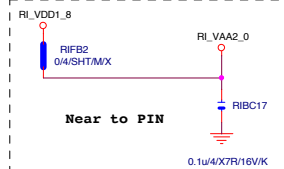
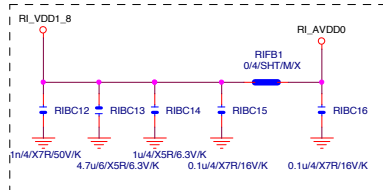
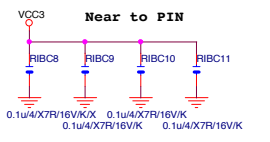
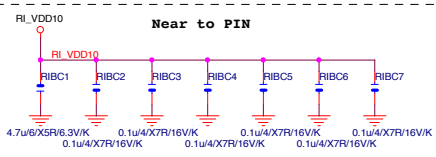


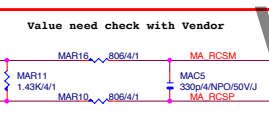
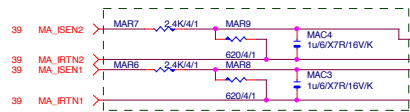
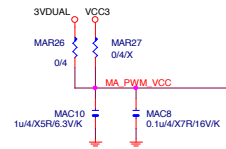
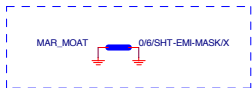
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1Gb	Orange
100Mb	Green
10Mb	Off





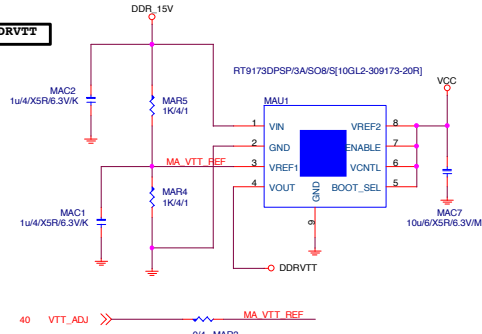


Close to DDR output inductor

should be routed as differential pair, 7mil width, 8mil spacing

40 DDR15V_ADJ1

DDRVTT

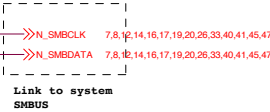


40 VTT_ADJ

IR3570

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MA_PWM2 39
MA_PWM1 39

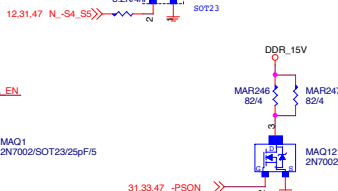
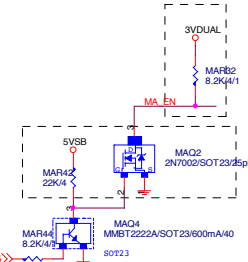


Addr: 72h

Link to PCB

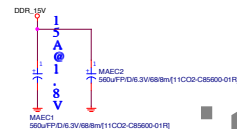
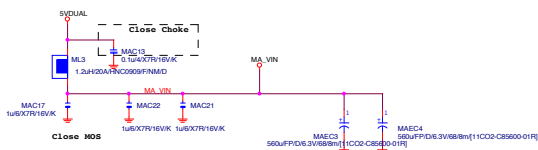
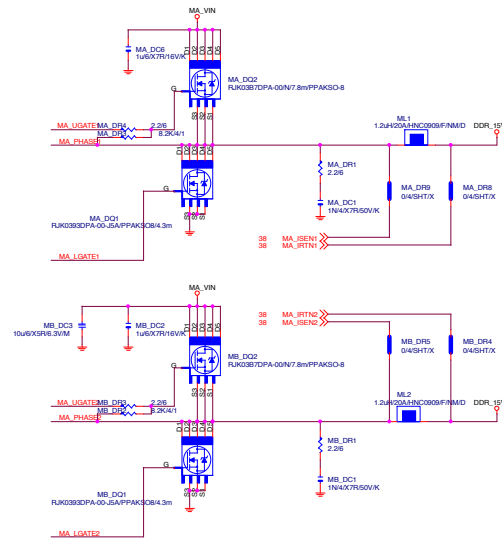
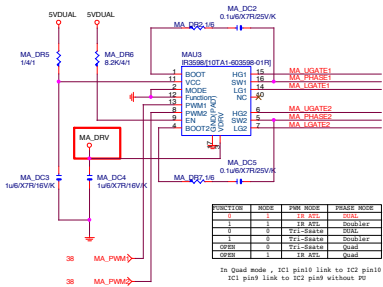
pin B046

Pull up in PCB side

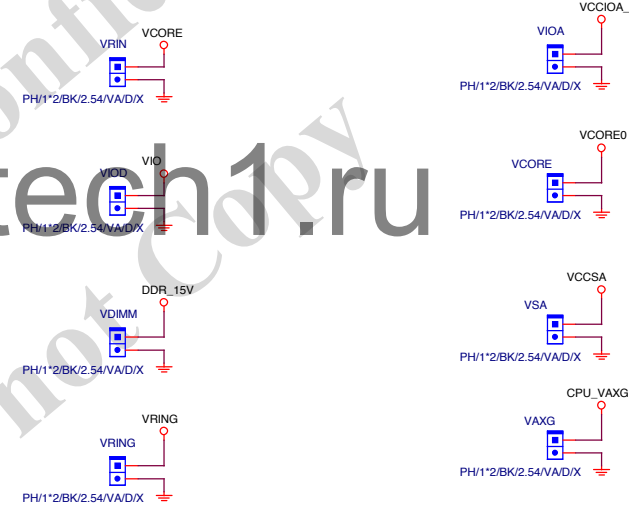
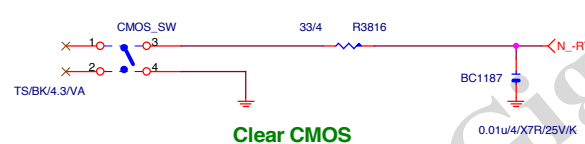
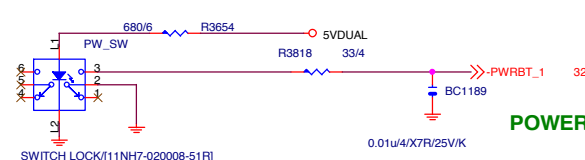
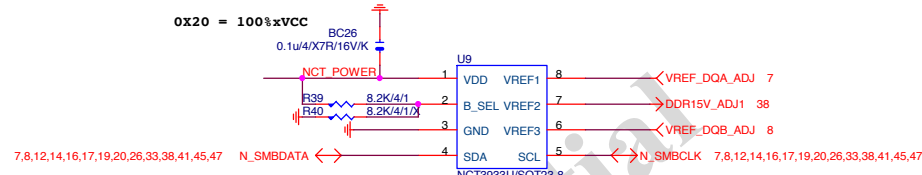
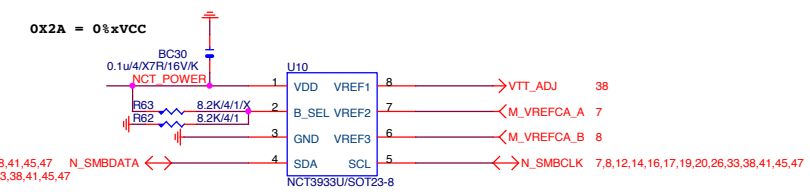
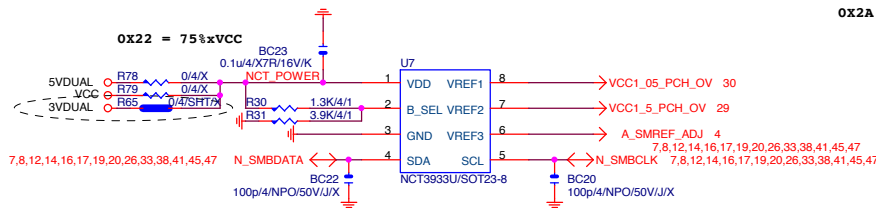


GIGABYTE™			
Title			
DDR POWER IR3570			
Size	Document Number	Rev	
C	G1.SNIPER5	1.02	
Date:	Tuesday, May 14, 2013	Sheet	38 of 55

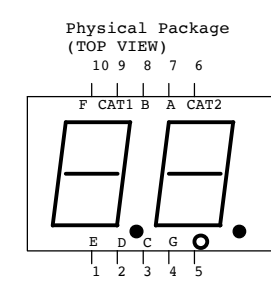
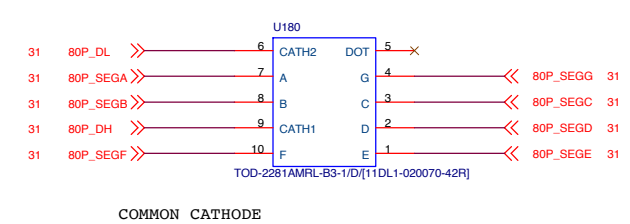
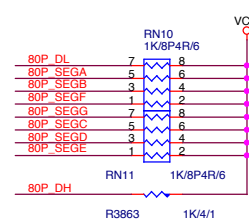
DDR_15V



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80 PORT

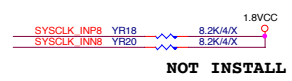
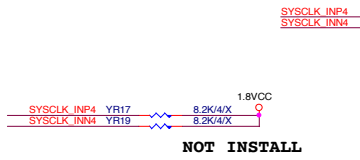


GIGABYTE™			
Title			
RST, PWR, CLR_CMOS			
Size	Document Number	Rev	
Custom	G1.SNIPER5	1.02	
Date:	Tuesday, May 14, 2013	Sheet	40 of 55

USB			
PA EXP A RXP0	V4	PEX_PERP16	V2
PA EXP A RXN0	V5	PEX_PERN16	V1
PA EXP A RXP1	U4	PEX_PERP17	U2
PA EXP A RXN1	U5	PEX_PERN17	U1
PA EXP A RXP2	R5	PEX_PERN18	R2
PA EXP A RXN2	R4	PEX_PERN19	R1
PA EXP A RXP3	P4	PEX_PERN20	P2
PA EXP A RXN3	P5	PEX_PERN21	P1
PA EXP A RXP4	M5	PEX_PERN22	M2
PA EXP A RXN4	M4	PEX_PERN23	M1
PA EXP A RXP5	L5	PEX_PERN24	L2
PA EXP A RXN5	L4	PEX_PERN25	L1
PA EXP A RXP6	J5	PEX_PERN26	J2
PA EXP A RXN6	J4	PEX_PERN27	J1
PA EXP A RXP7	H5	PEX_PERN28	H2
PA EXP A RXN7	H4	PEX_PERN29	H1
PA EXP A RXP8	D1	PEX_PERN30	D2
PA EXP A RXN8	D2	PEX_PERN31	D1
PA EXP A RXP9	E4	PEX_PERN32	E2
PA EXP A RXN9	E5	PEX_PERN33	E1
PA EXP A RXP10	D4	PEX_PERN34	D2
PA EXP A RXN10	D5	PEX_PERN35	D1
PA EXP A RXP11	E7	PEX_PERN36	E2
PA EXP A RXN11	E8	PEX_PERN37	E1
PA EXP A RXP12	D7	PEX_PERN38	D2
PA EXP A RXN12	D8	PEX_PERN39	D1
PA EXP A RXP13	E10	PEX_PERN40	E2
PA EXP A RXN13	E11	PEX_PERN41	E1
PA EXP A RXP14	D10	PEX_PERN42	D2
PA EXP A RXN14	D11	PEX_PERN43	D1
PA EXP A RXP15	E11	PEX_PERN44	E2
PA EXP A RXN15	D11	PEX_PERN45	D1
PEX_PERP32	V22	PEX_PERN46	P2
PEX_PERN32	V23	PEX_PERN47	P1
PEX_PERP33	U22	PEX_PERN48	U2
PEX_PERN33	U23	PEX_PERN49	U1
PEX_PERP34	R22	PEX_PERN50	R2
PEX_PERN34	R23	PEX_PERN51	R1
PEX_PERP35	P22	PEX_PERN52	P2
PEX_PERN35	P23	PEX_PERN53	P1
PEX_PERP36	M22	PEX_PERN54	M2
PEX_PERN36	M23	PEX_PERN55	M1
PEX_PERP37	L22	PEX_PERN56	L2
PEX_PERN37	L23	PEX_PERN57	L1
PEX_PERP38	J22	PEX_PERN58	J2
PEX_PERN38	J23	PEX_PERN59	J1
PEX_PERP39	H22	PEX_PERN60	H2
PEX_PERN39	H23	PEX_PERN61	H1
PEX_PERP40	D22	PEX_PERN62	D2
PEX_PERN40	D23	PEX_PERN63	D1
PEX_PERP41	E22	PEX_PERN64	E2
PEX_PERN41	E23	PEX_PERN65	E1
PEX_PERP42	D20	PEX_PERN66	D2
PEX_PERN42	D21	PEX_PERN67	D1
PEX_PERP43	E19	PEX_PERN68	E2
PEX_PERN43	E20	PEX_PERN69	E1
PEX_PERP44	D17	PEX_PERN70	D2
PEX_PERN44	D18	PEX_PERN71	D1
PEX_PERP45	E16	PEX_PERN72	E2
PEX_PERN45	E17	PEX_PERN73	E1
PEX_PERP46	D14	PEX_PERN74	D2
PEX_PERN46	D15	PEX_PERN75	D1
PEX_PERP47	E13	PEX_PERN76	E2
PEX_PERN47	E14	PEX_PERN77	E1

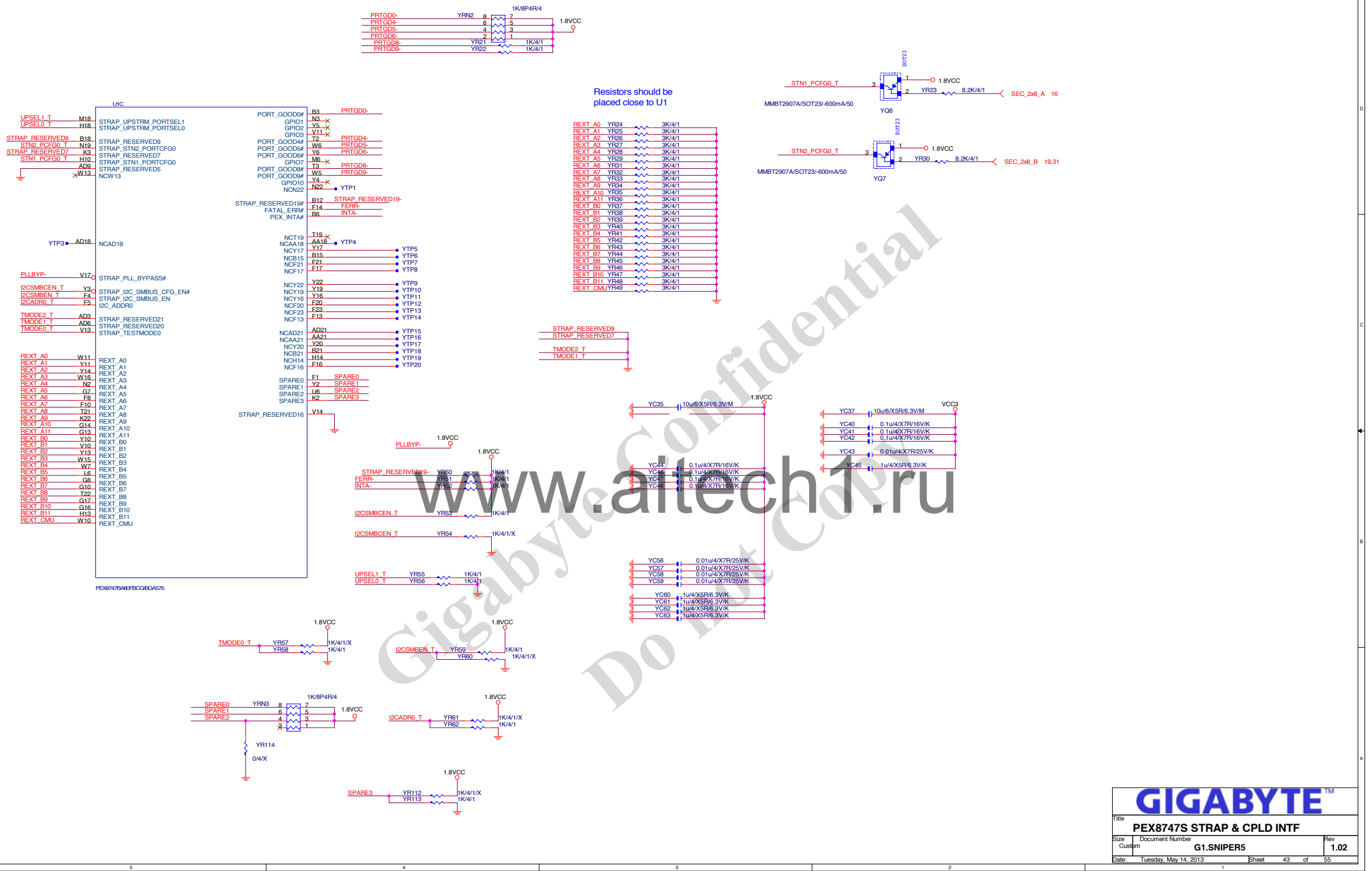
PA EXP A RXP0.71	>>>PA_EXP_A_RXP[0..7]	15
PA EXP A RXN0.71	>>>PA_EXP_A_RXN[0..7]	15
PA EXP A TXP0.71	>>>PA_EXP_A_TXP[0..7]	15
PA EXP A TXN0.71	>>>PA_EXP_A_TXN[0..7]	15
PA EXP A RXP8.15	>>>PA_EXP_A_RXP[8..15]	14
PA EXP A RXN8.15	>>>PA_EXP_A_RXN[8..15]	14
PA EXP A TXP8.15	>>>PA_EXP_A_TXP[8..15]	14
PA EXP A TXN8.15	>>>PA_EXP_A_TXN[8..15]	14
PB EXP B RXP0.71	>>>PB_EXP_B_RXP[0..7]	17
PB EXP B RXN0.71	>>>PB_EXP_B_RXN[0..7]	17
PB EXP B TXP0.71	>>>PB_EXP_B_TXP[0..7]	17
PB EXP B TXN0.71	>>>PB_EXP_B_TXN[0..7]	17
PB EXP B RXP8.15	>>>PB_EXP_B_RXP[8..15]	18
PB EXP B RXN8.15	>>>PB_EXP_B_RXN[8..15]	18
PB EXP B TXP8.15	>>>PB_EXP_B_TXP[8..15]	18
PB EXP B TXN8.15	>>>PB_EXP_B_TXN[8..15]	18

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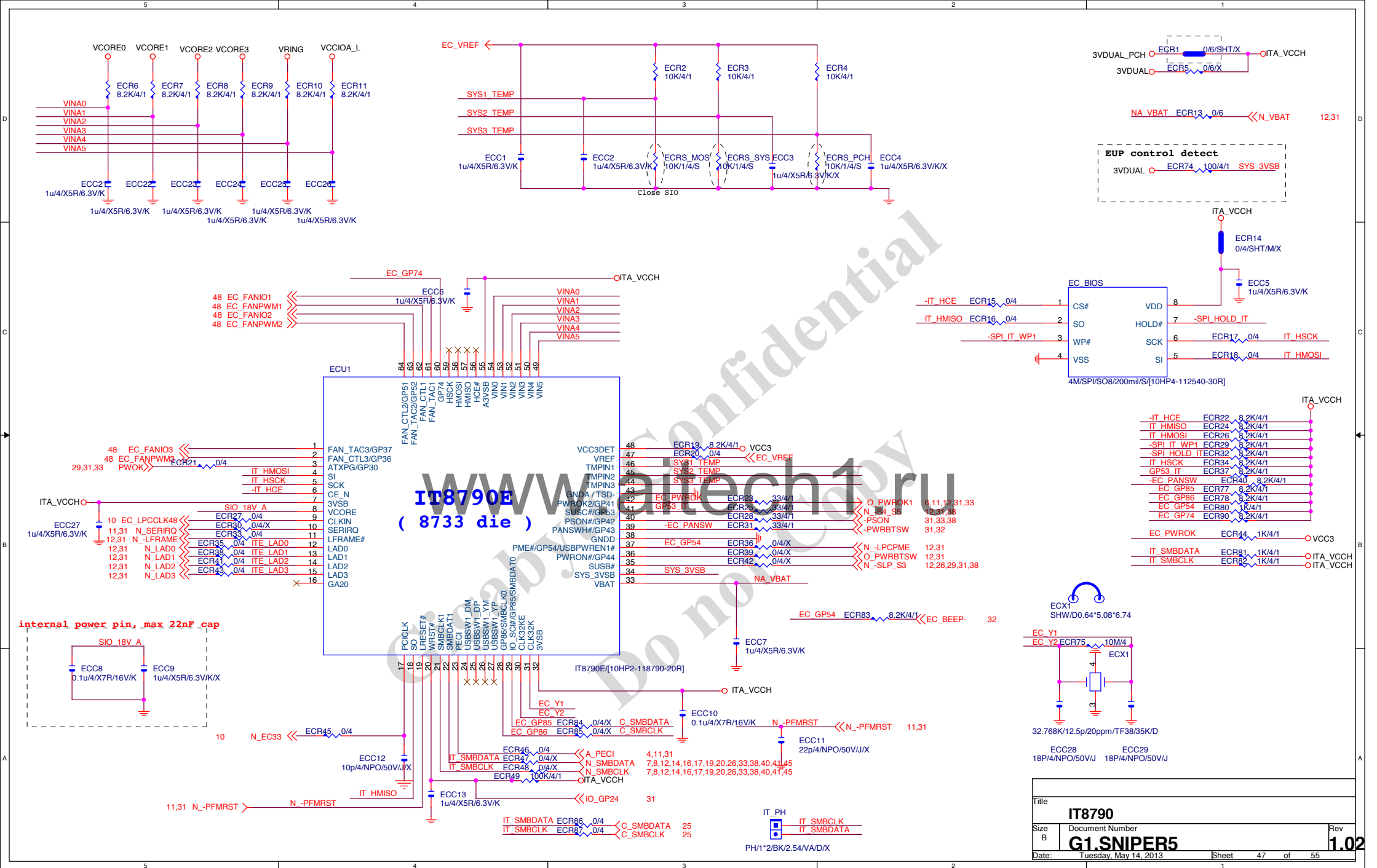


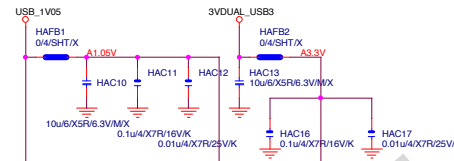
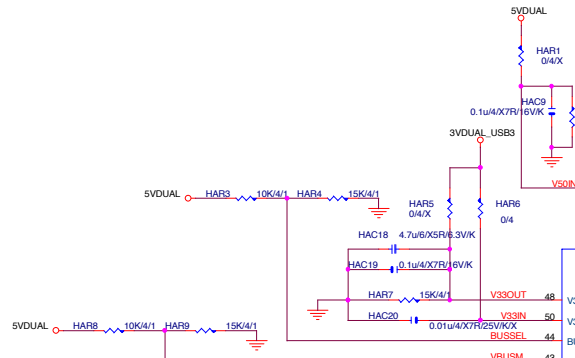
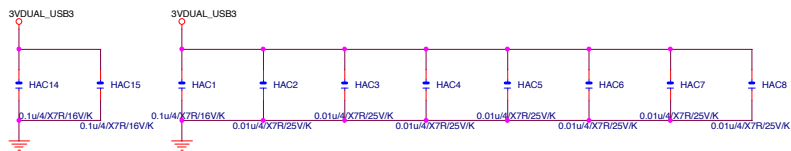
GIGABYTE™

Title PEX8747S DOWNSTREAM SLOTS		
Size Custom	Document Number G1.SNIPER5	Rev 1.02
Date Tuesday, May 14, 2013	Sheet 42	of 55

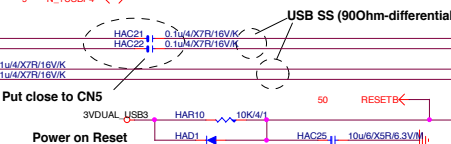




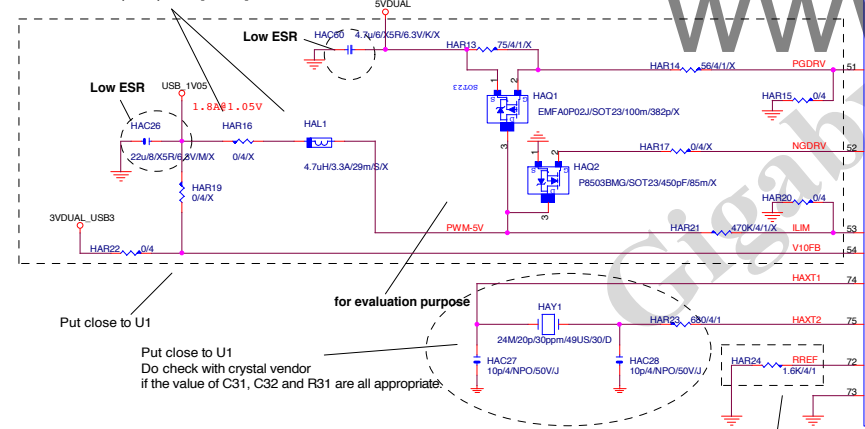




From PCH
9 PCH_USB3_RXN4
9 PCH_USB3_RXP4
9 PCH_USB3_TXN4
9 PCH_USB3_TXP4



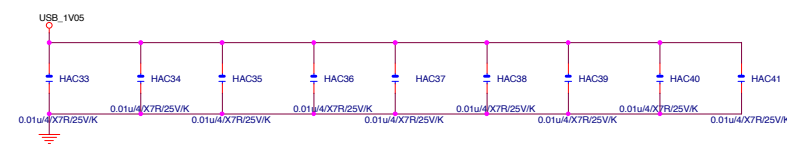
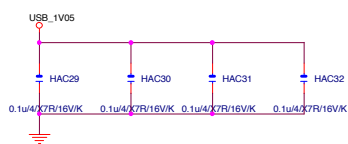
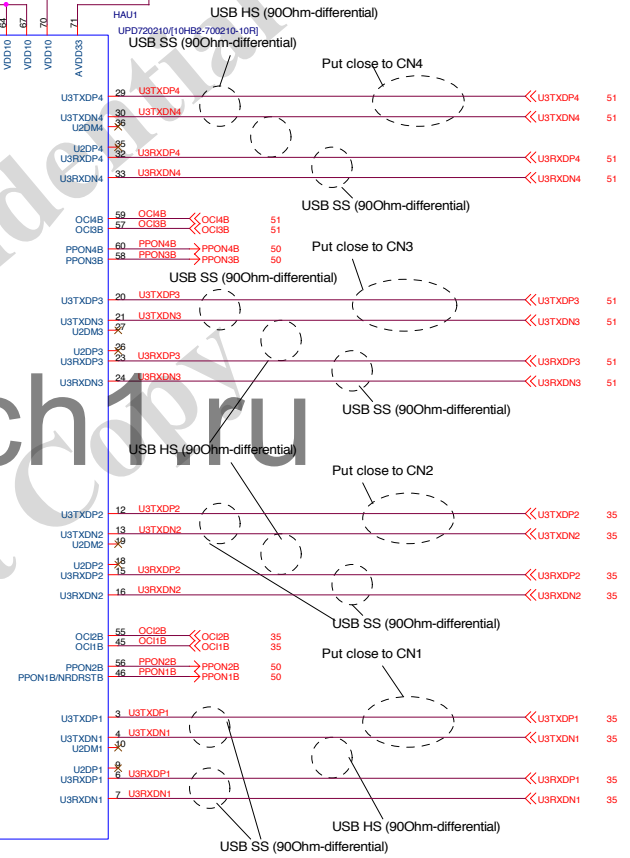
The over current protection of VDD10 is detected with ILIM pin (No.53) using 180 mOhm of DC resistance (DCR) of inductor L1.
HAR16 should be choosing so that the total resistance of DCR(L1) becomes 180 mOhm.
→ HAR16 + DCR(HAL1) = 180 [mOhm]



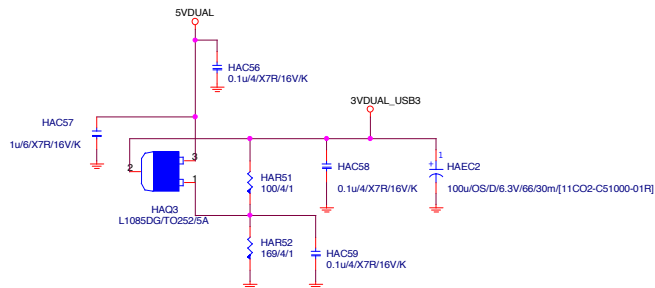
Put close to U1
Do check with crystal vendor
if the value of C31, C32 and R31 are all appropriate.

Put close to U1
Short and broad connection to GND
Don't split R32 into multiple resistors.

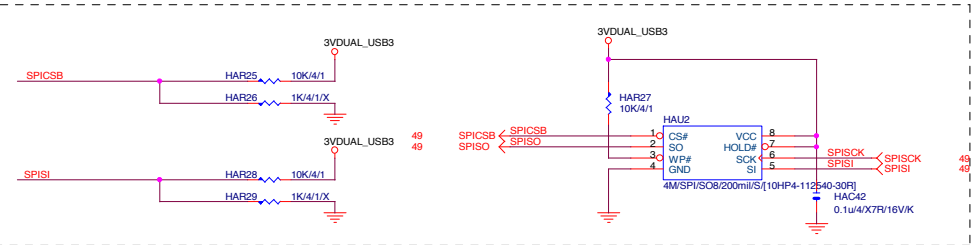
uPD720210



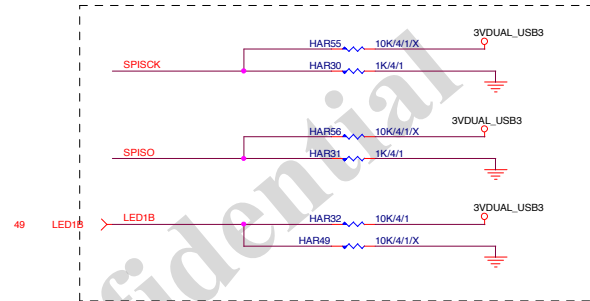
3VDUAL_USB_1



External SPI ROM ; SPI ROM attached mode

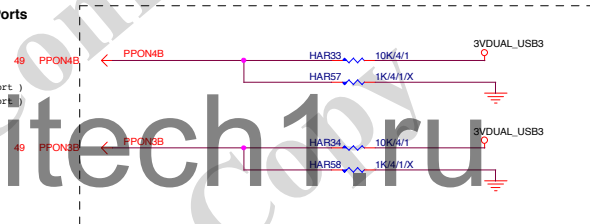


Battery Charging

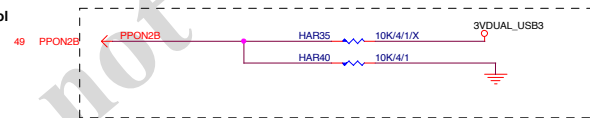


Number of Ports ; 4Ports mode

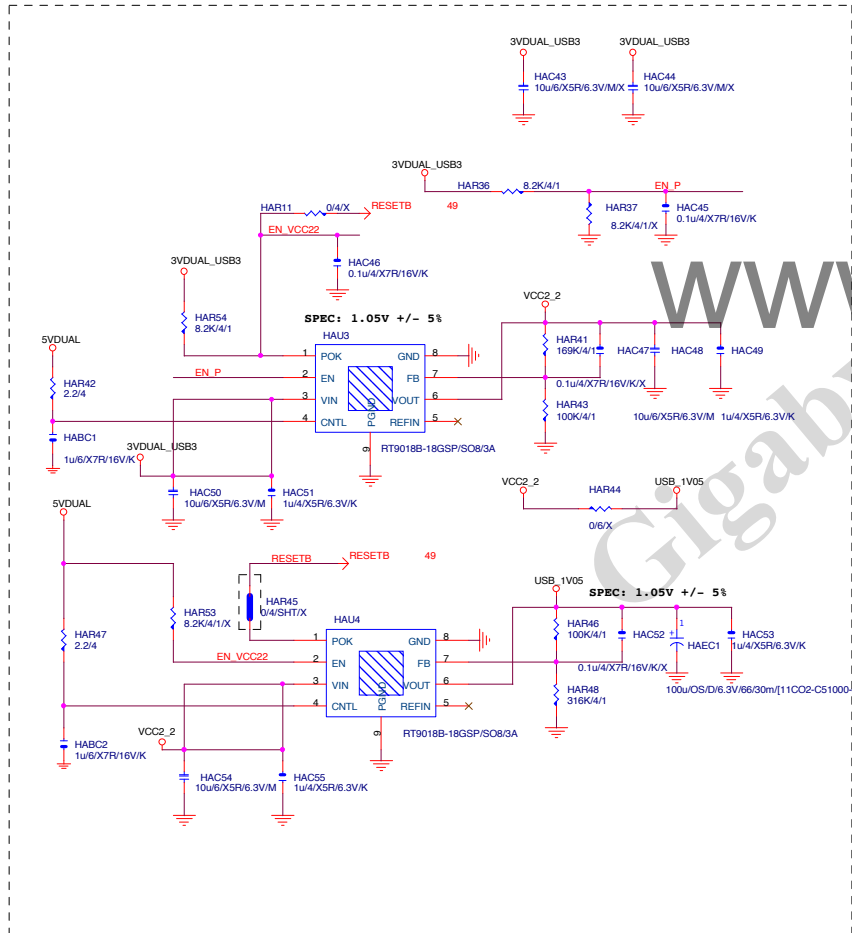
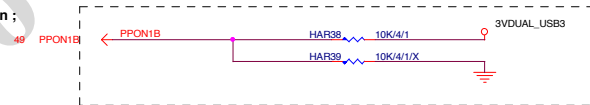
PPON3B / PPON4B : B / B (4 port)
PPON3B / PPON4B : L / L (2 port)



#5 VBUS Power Control ; Individual mode

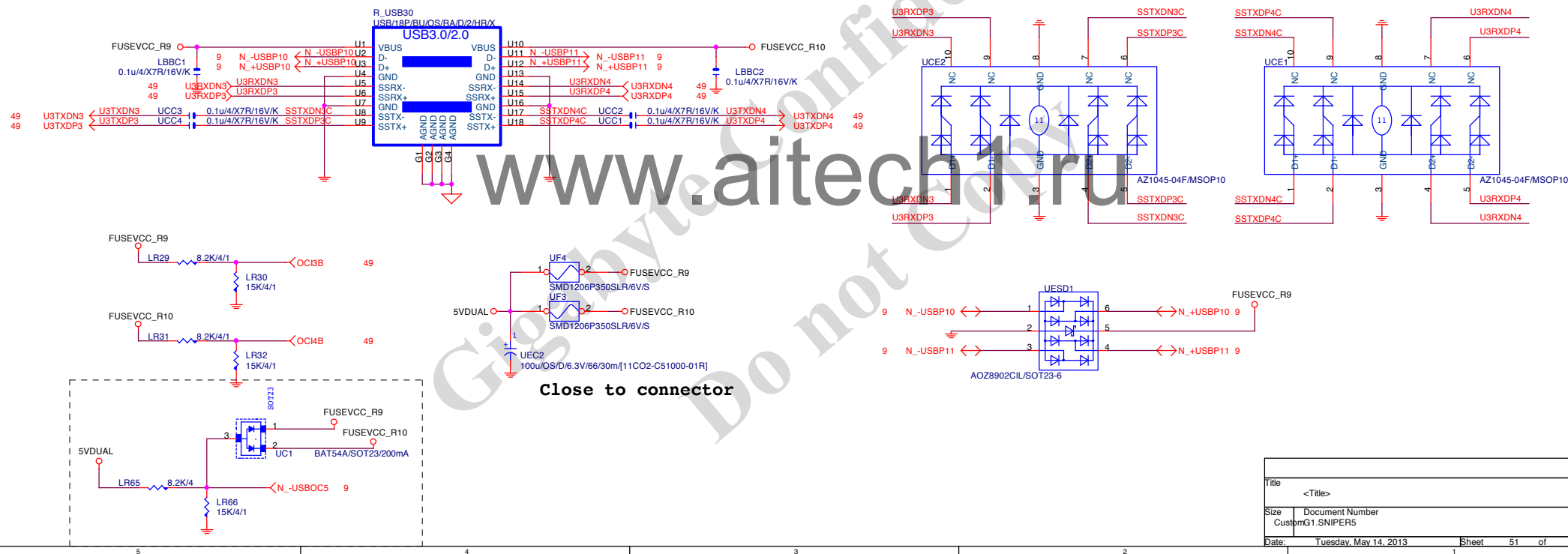


PPON1B Pin Function ; Port1 PPONB mode

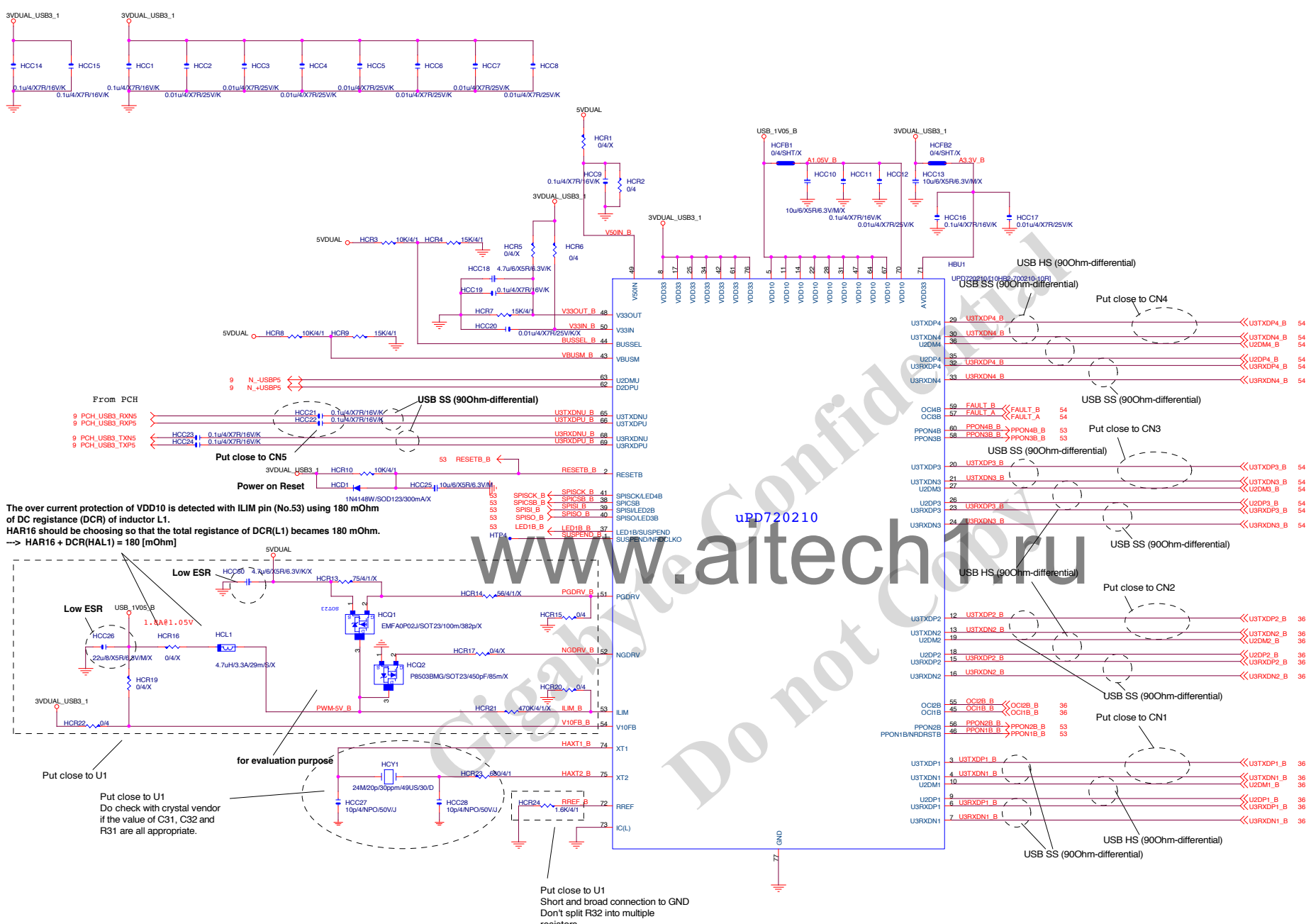


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Title		UPD720210 reference design 4port Hub board	
Size	Document Number	Rev	1.02
Date	Sheet	50	of



Title		
<Title>		
Size	Document Number	Rev
Custom	G1.SNIPER5	1.02
Date	Tuesday, May 14, 2013	Sheet 51 of 55



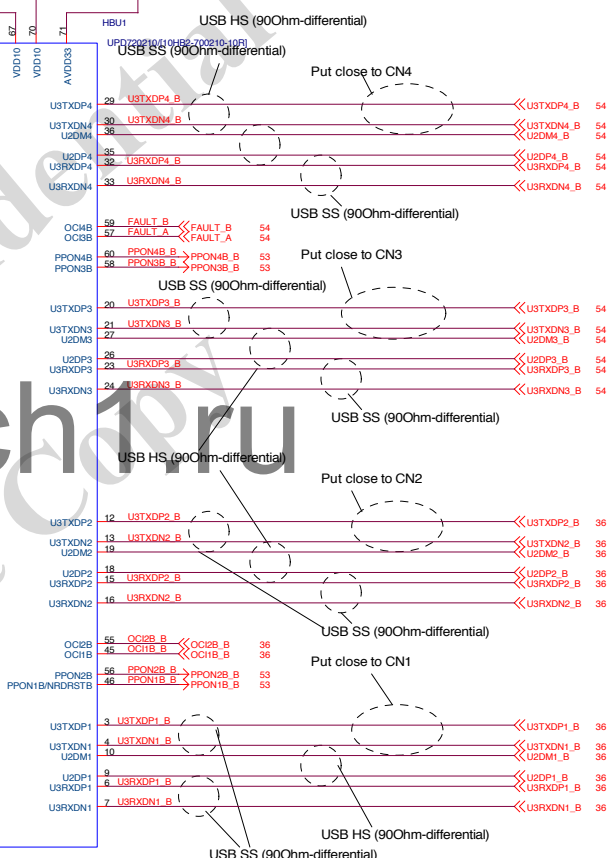
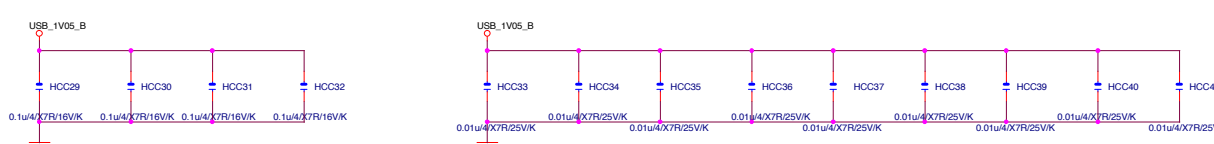
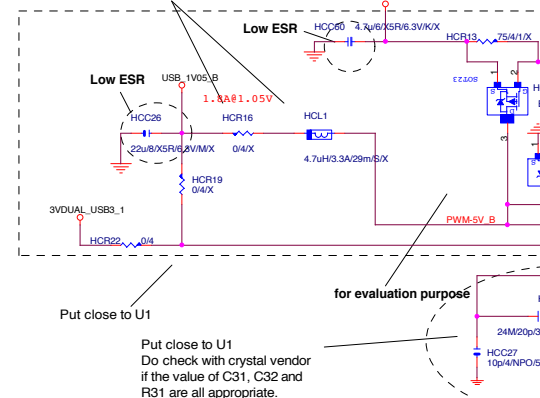
From PCH
9 PCH_USB3_RXN5
9 PCH_USB3_RXP5
9 PCH_USB3_TXN5
9 PCH_USB3_TXP5

Put close to CN5

USB SS (90Ohm-differential)

Power on Reset

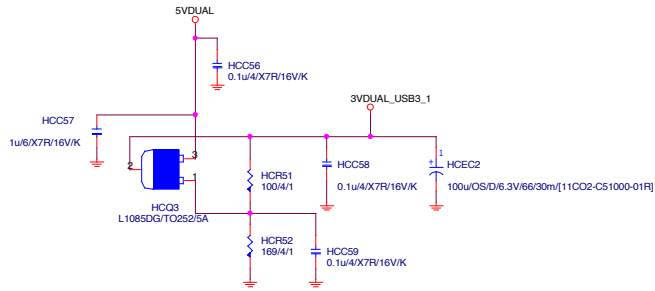
The over current protection of VDD10 is detected with ILIM pin (No.53) using 180 mOhm of DC resistance (DCR) of inductor L1.
HAR16 should be choosing so that the total resistance of DCR(L1) becomes 180 mOhm.
→ HAR16 + DCR(HAL1) = 180 [mOhm]



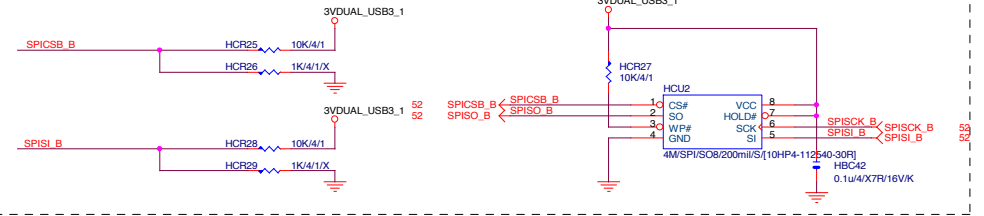
Put close to U1
Short and broad connection to GND
Don't split R32 into multiple resistors.

Title			
<Title>			
Size	Document Number	ISG-NK1-110006	1.02
C	G1.SNIPERS		
Date	Tuesday, 10/10/2018	Sheet	52 of 85

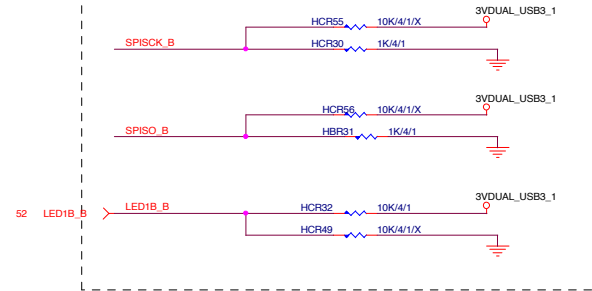
3VDUAL_USB_2



External SPI ROM ; SPI ROM attached mode

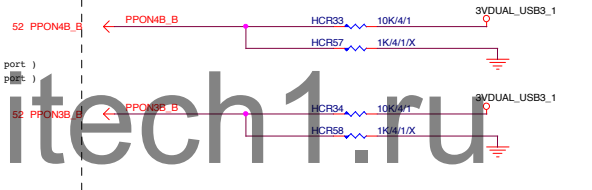


Battery Charging

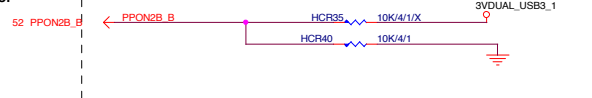


Number of Ports ; 4Ports mode

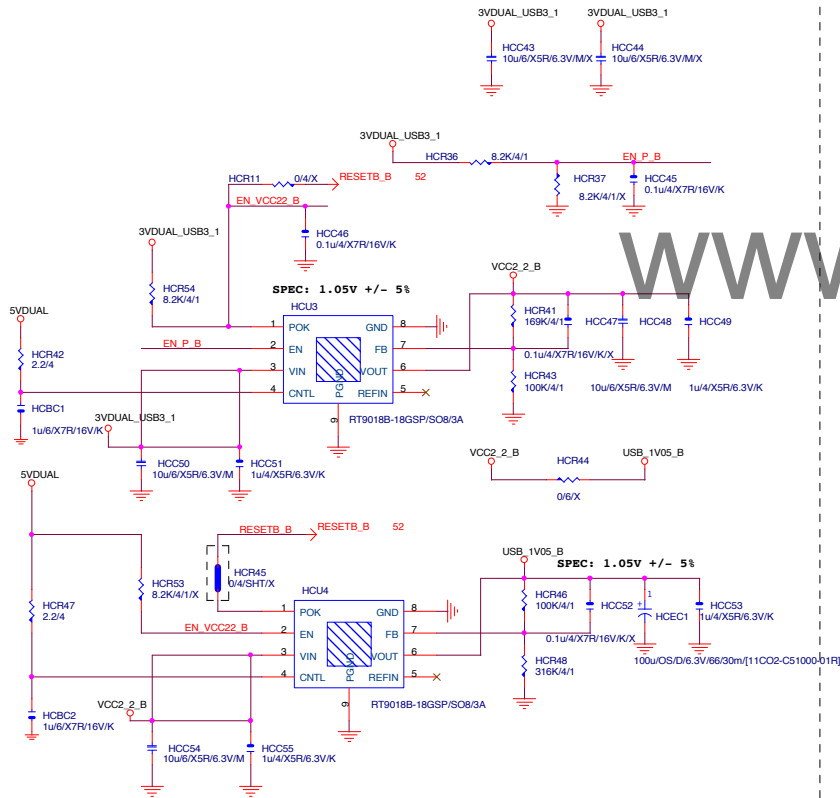
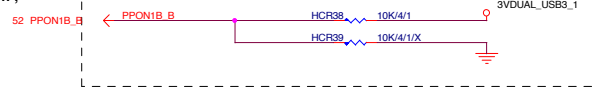
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)



#5 VBUS Power Control ; Individual mode

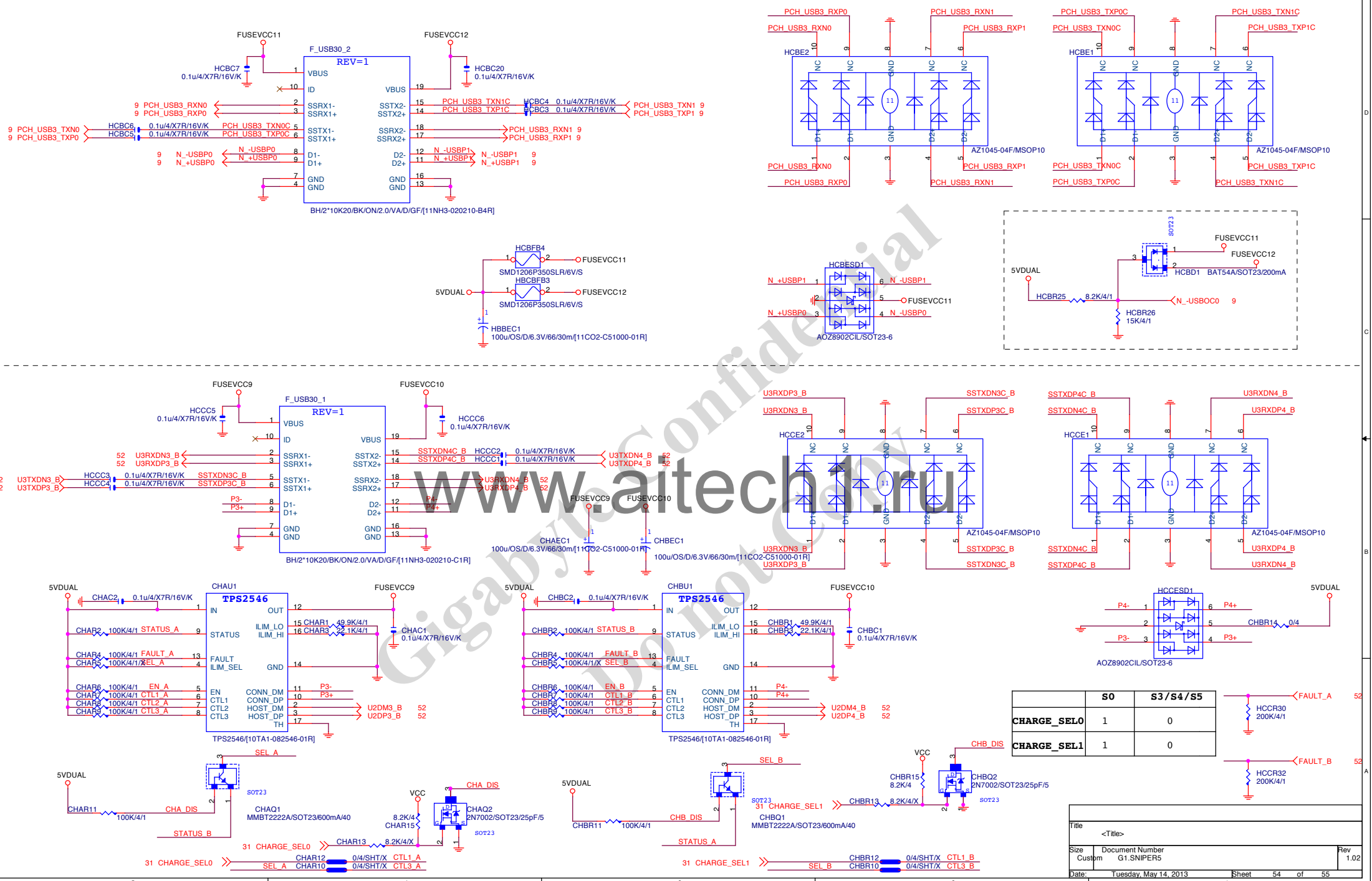


PPON1B Pin Function ; Port1 PPONB mode



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Title		UPD720210 reference design 4port Hub board	
Size	Document Number	Rev	1.02
Date	Sheet	53	of



	S0	S3/S4/S5	
CHARGE_SELO	1	0	
CHARGE_SEL1	1	0	

Title	<Title>		
Size	Custom	Document Number	Rev
		G1.SNIPERS	1.02
Date:	Tuesday, May 14, 2013	Sheet	54 of 55

5

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2

2

22